CFP8 MDIO Proposal

CFP MSA Member Companies:
Finisar Corp.
Foxconn Interconnect Technology Ltd.
Fujitsu Optical Components
Lumentum Operations LLC
NeoPhotonics Corp.
Oclaro, Inc.
Sumitomo Electric Industries, Ltd.

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Introduction

- This is a proposal for MDIO interface for CFP8 based on Baseline and Optional requirements below.
- In CFP8, MOD_SELn pin replaces PRTADR pins for module select. Detail specifications and procedures are described in following pages for each case.
- Baseline: dedicated MDIO bus for each module (required)
  - No host intervention required. MOD_SELn pin is unused, can be no connect on the host. Host addresses the module by using power-up and reset default
- Optional: MDIO bus with multiple modules (optional)
  - On power-up or after reset, the host asserts MOD_SELn pin which overrides the internal address. i.e. the module responds to any address. This enables the host to write unique module addresses.

Management Interface Pins

Table 1. Management Interface Pins (MDIO)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Term.
89	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
91	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
92	MDC	MDIO Clock	I	1.2V LVCMOS			
90	MOD_SELn	Module Select (invert)	I	3.3V LVCMOS	De-selected	Selected	Pull-Up

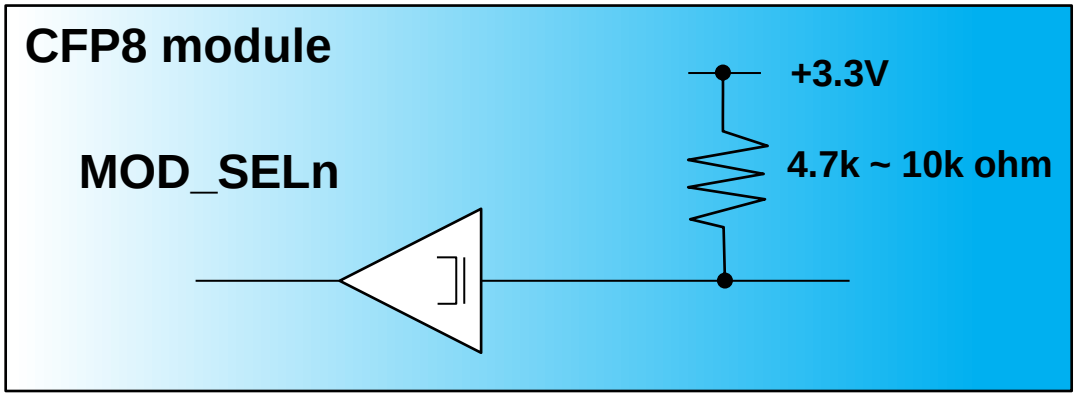


Figure 1. Reference +3.3V LVCMOS Input Termination

Baseline: Dedicated MDIO Bus for each Module

- Initial PHYADR value in CFP8 is 5b’00000. CFP8 comes out of power-up or reset with the default address and responds to any MDIO command with this default address.
- Host intervention is not required. MOD_SELn pin is unused, and can be no connect on the host.

Optional: MDIO bus with multiple modules

- Initial PHYADR value in CFP8 is 5b'00000. CFP8 comes out of power-up or reset with the default address and normally responds to any MDIO command.
- Hosts that use a shared MDIO bus have to assert MOD_SELn to individually set the module addresses as follows. (Note 1)
- Host asserts MOD_SELn before setting a new PHYADR to target CFP8.
- When host asserts MOD_SELn pin, the module responds to any operation code (i.e. OP=00/01/10/11) on the MDIO bus. Any PHYADR is valid. CFP8 PHYADR is changed to to the received PHYADR.
- Once the new PHYADR is changed, CFP8 retains the PHYADR until power-off, reset, or reprogramming during next MOD_RSTs assertion.

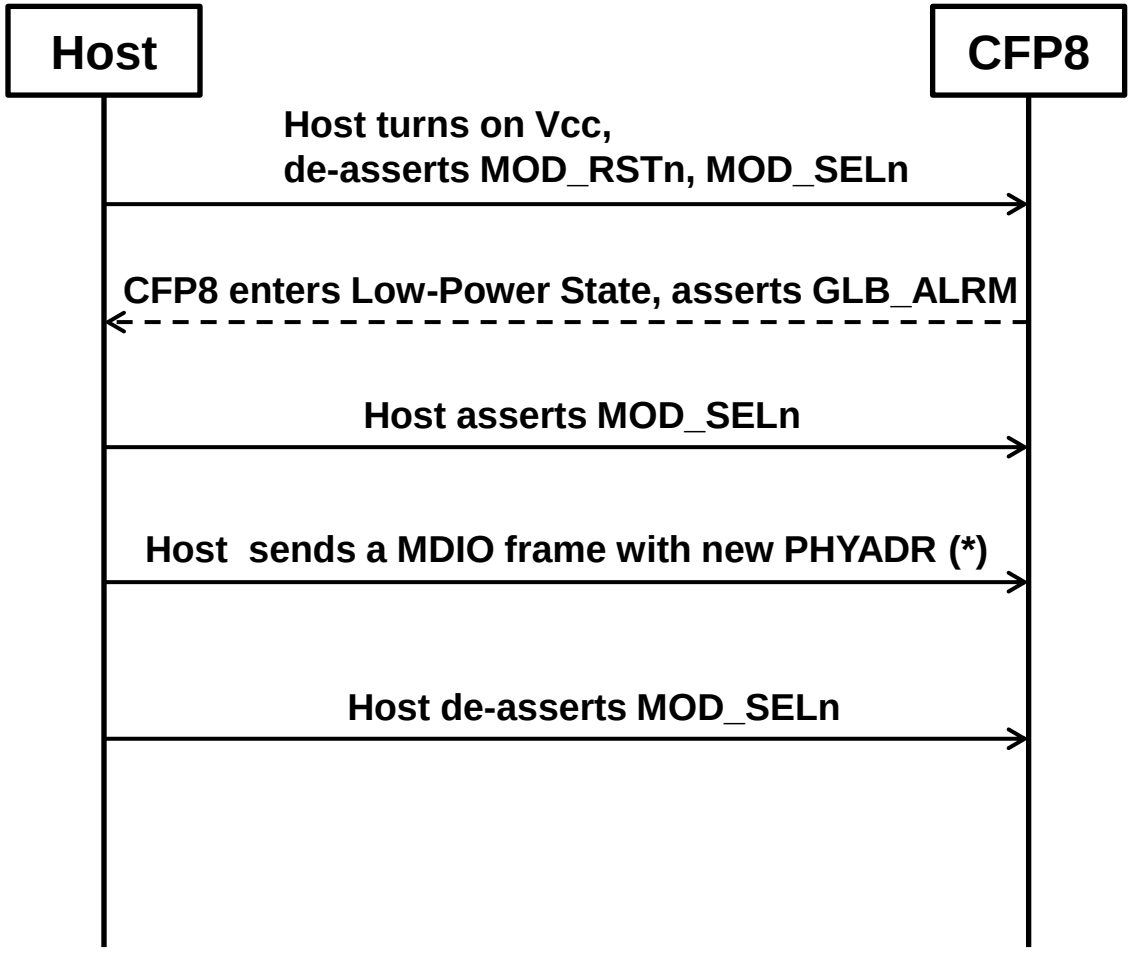
Figure 2. CFP8 MDIO Management Frame Structure

Note1: MOD_SELn asserted means the MOD_SELn pin is set low and the module is selected. MOD_SELn de-assert means the MOD_SELn pin set thigh and the module is de-selected.
Note2: When the MOD_SELn is asserted, data following PHYADR (i.e. DEVADR, TA and 16-bit ADDRESS/DATA is neglected regardless of the operation code.

Warning

- In multiple modules on MDIO bus implementations, when the module comes out from power-up or reset, including after being plugged into an operating board, the host must insure that there is no bus contention conflict. For example, the host cannot use default address 5b’00000 because it will result in multiple modules responding.

Optional: PHYADR Setup Sequence



(*) With any operation code; 00/01/10/11.

Figure 3. PHYADR setup sequence

Optional: MOD_SELn Timing Diagram

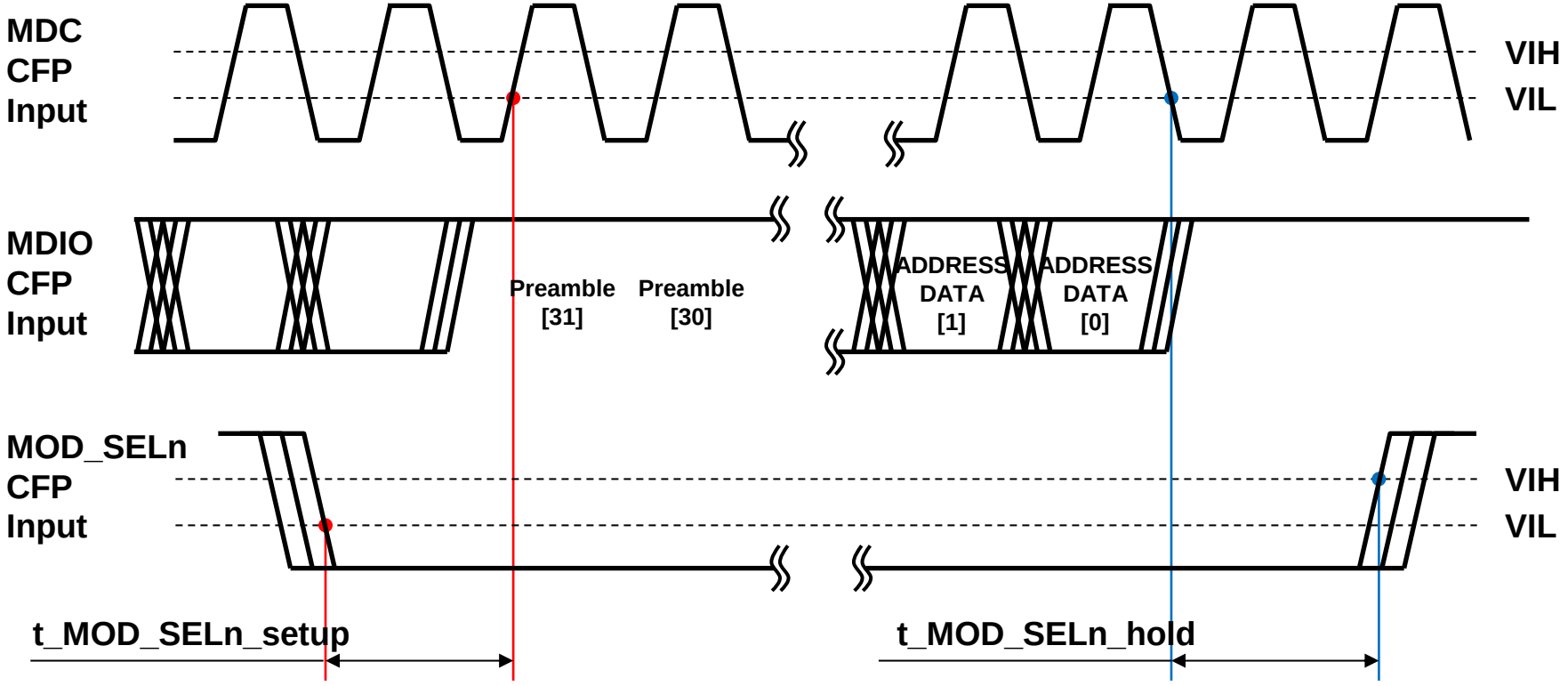


Figure 4. MOD_SELn & MDC Timing Diagram

Optional: MOD_SELn Timing Parameters

Table 2. Timing Parameters for CFP8 Hardware Signal Pins

Parameter	Symbol	Min.	Max.	Unit	Notes & Condition
Host MOD_SELn Setup Time	t_MOD_SELn_setup	100	-	ms	Before the rising edge of MDC clock cycle for the first preamble bit.
Host MOD_SELn Hold Time	t_MOD_SELn_hold	1	-	ms	After the falling edge of MDC clock cycle for the last ADDRESS/DATA bit.

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Thank you