Addendums to CFP MSA MIS V2.2r06a

To be integrated into CFP MSA MIS Future Publication

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1 REVISION HISTORY

Revision	Date	Objective	By
0.1	*03/03/2014*	*Draft for CFP MSA review.*	*Jiashu Chen*
0.2	*07/21/2014*	*Draft for CFP MSA review*	*Jiashu Chen*
0.3	*07/21/2014*	*Draft for CFP MSA review*	*Jiashu Chen*
0.4a	*09/06/2014*	*Draft for CFP MSA review*	*Jiashu Chen*
0.5b	*11/06/2014*	*Draft for Broad Group Review*	*Jiashu Chen*
0.5c	*11/07/2014*	*Updated draft for Broad Group Review*	*Jiashu Chen*
1.0	*11/15/2014*	*CFP-MSA Website Publication*	*Jiashu Chen*
1.0r1	*11/20/2014*	*CFP-MSA Website Publication, typo corrections on page 18 line 20 "host" to "network". "Draft…" on cover page is also removed.*	*Jiashu Chen*

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ADDENDUMS TO CFP MSA MIS V2.2R06A

This section of document contains addendums to CFP MSA MIS V2.2 r06a as the interim publication prior to CFP MSA MIS V2.4. After review and approval these addendums shall be integrated into the publication of V2.4 properly. These addendums are extracted from CFP MSA MIS V2.2 Review Comment Form and are deemed to be ready for formal publication for MIS V2.4.

1 ADDENDUM 1 - DEFINING SIGNAL EQUALIZATION AND SIGNAL PRE/DE-EMPHASIS BITS IN A440H AND B640H

1.1 Reference

Keywords	IEEE802.3bm CAUI-4 Spec., Signal Equalization, Register A440h, Register B640h
To CFP MSA MIS V2.2r06a	Page 103 A440h. Page 154 B640h
To CFP MSA MIS Comment Log	Juniper 8, 12, 13, 14, Finisar 50, JDSU 6, ALU 7.

1.2 Problem Description

This Addendum is to address the following problems raised in respective comments.

1. At present, the CFP MSA leaves support for CEI-28G-VSR to be "vendor specific." This is not acceptable as a means for fostering broad market potential for this electrical interface. We need "plug and play." The OIF has been taking up the task of improving the definition to account for a uniform means of configuring modules that adopt CEI-28G-VSR. This will be valid for all MSAs that adopt the use of CEI-28G-VSR. It is possible that the IEEE will actually define the register for the control as part of CAUI-4.
2. Note that CAUI-4 only requires CTLE settings from the host ranging from 1 dB to 9 dB.
3. No default CAUI-4 CTLE setting is defined.
4. CAUI-4 does not require the use of pre/de-emphasis yet some module integrators support its use. There is no defined default setting for pre/de-emphasis in the context of CAUI-4. Some vendors are interpreting the 3.5 dB default value of CAUI-10 to apply to CAUI-4, which creates a signaling problem when the host software does not configure the pre/de-emphasis setting.

1.3 Solution

1. Adding 5-bit field A440h.12~9 for supporting Signal Equalization Gain. Bits 12~9 map provide total 16 codes to match IEEE802.3bm CTLE specification.
2. Modifying Description of A440h.12~9 to reserve some codes for IEEE802.3bm compatibility. Bit 8 is added to support some device backward compatibility for 0.5 dB increment.
3. Setting A440h.12~8 initial value to 000010b
4. Similar changes are made to B640h but note the bit mapping is different.
5. For CAUI-4, the default value of pre/de-emphasis (if supported) needs to be 0 dB. The currently indicated 3.5 dB default needs to be identified as only pertaining to CAUI-10.
6. The details of the solutions are implemented in the following registers.

1

Host Lane Control Registers						
A440	**16**			**Host Lane m Control**	**16 registers, one for each host lane, represent 16 host lanes. m = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0007h**
		RW	15	Signal equalization mode control	0: Automatic, 1: Manual.	0
		RO	14~13	Reserved		0
		RW	12~8	Signal Equalization Gain	A total 5-bit unsigned filed is defined to support Signal Equalization Gain. Of the 5 bits, bits 12~9 map to the 4-bit code defined by IEEE802.3bm representing the CTLE equalization gain at 14 GHz relative to 0.1 GHz. Out of 16 available codes, 1, 2, 3, …, 9 match CTLE code 1 through 9 dB settings. To be compatible with IEEE802.3bm, the following codes are reserved: 1111b, 1110b, 1101b, 1100b, 1011b, 1010b. Code 0000b is intended for Vendor Specific subject to negotiation with IEEE. For some device backward compatibility bit 8 is allocated to represent a 0.5 dB increment to CTLE setting.	0
		RW	3~0	Signal Pre/De-emphasis	4-bit unsigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = N * 0.5 dB, N = 0, …, 15. The power on initial value is 3.5 dB with a value of 7 in this field for CAUI-10. Initial value for CAUI-4 is 0 dB.	7

2

Host Lane Control Registers						
B640 [2.0]	**16**			**Host Lane m Control**	**16 registers, one for each host lane, represent 16 host lanes. n = 0, 1, …, M-1. M_max = 16. Actual M is module dependent.**	**0007h**
		RO	15~12	Reserved		0
		RW	11	Signal equalization mode control	0: Automatic, 1: Manual.	0
			8~4	Signal Equalization Gain	A total 5-bit unsigned filed is defined to support Signal Equalization Gain. Of the 5 bits, bits 8~5 maps to the 4-bit code defined by IEEE802.3bm representing the CTLE equalization gain at 14 GHz relative to 0.1 GHz. Out of 16 available codes, 1, 2, 3, …, 9 match CTLE code 1 through 9 dB settings. To be compatible with IEEE802.3bm, the following codes are reserved: 1111b, 1110b, 1101b, 1100b, 1011b, and 1010b. Code 0000b is intended for Vendor Specific subject to negotiation with IEEE. For some device backward compatibility bit 4 is allocated to represent a 0.5 dB increment to CTLE setting.	0
		RW	3~0	Signal Pre/De-emphasis	4-bit unsigned number N represents the pre/de-emphasis applied. Pre/De-emphasis = N * 0.5 dB, N = 0, …, 15. The power on initial value is 3.5 dB with a value of 7 in this field for CAUI-10. Initial value for CAUI-4 is 0 dB.	7

3 ## 1.4 Editor's Remark and Additional Proposal

4 None.

2 ADDENDUM 2 ADDING CFP4 PINOUT SCHEME SELECT TO 807EH AND A015H

2.1 Reference

Keywords	**CFP4 Host Lane Pin-out Type**
To CFP MSA MIS V2.2r06a	**CFP NVR and VR registers, 807Eh and A015h**
To CFP MSA MIS Comment Log	**Finisar 52**

2.2 Problem Description

We need a method in CFP4 to define which type of module is implemented and if it is programmable, and a method for doing that programming.

2.3 Solution

See the changes below (highlighted in yellow):

807E [2.2]	**1**	RO		**CFP and CFP2/4 Extended Identifier**		
			4	CFP4 Host Lane Pin-out Type	0b: Fixed, 1b: Programmable via A015h.8, (optional).	0
			2~0	Reserved		0

A015 [2.2]	**1**	**RW**		**Module General Control 2**	**This register collects added module general control functions for CFP MSA MIS V2.2**	**0000h**
			8	CFP4 Host Lane Pin-out Select	0b: TOP if 807Eh.4 = 1b 1b: TOP ALT1 if 807Eh.4 = 1b, No effect if 807Eh.4 = 0b	0

B015 [2.2]	**1**	**RW**		**Module General Control 2**	**This register collects added module general control functions for CFP MSA MIS V2.2**	**0000h**
			8	CFP4 Host Lane Pin-out Select	0b: TOP if 807Eh.4 = 1b 1b: TOP ALT1 if 807Eh.4 = 1b, No effect if 807Eh.4 = 0b	0

2.4 Editor's Remark and Additional Proposal

Currently there is no coherent module in the CFP4 form factor proposed. Therefore, the mockup of register B015h.8 is for place holding.

3 ADDENDUM 3 MODIFYING CFP4 PROGRAMMABLE PINS

3.1 Reference

Keywords	CFP4, TX_DIS pin, RX_LOS pin, Programmable control pin, programmable alarm pin.
To CFP MSA MIS V2.2r06a	Register A007h
To CFP MSA MIS Comment Log	Sumitomo 7

3.2 Problem Description

1. CFP4 Pin Allocation (Pin Allocation Rev. 25) specifies that the user can use TX_DIS pin as Programmable control pin after the user configures some registers and resets the module. There is a similar description on RX_LOS pin. However, current MIS document does not describe the registers and definitions to be able to do that.

2. There is no MDIO register to define whether the module supports the hardware PRG_CNTL1 and PRG_ALRM1 configuration or not in NVR region.

3.3 Solution

1. Add code 10 to program these two pins as TX_DIS and RX_LOS for CFP4 modules.
2. Add bit 807Eh.3 to indicate the option of TxDIS or PRG_CNTL1, 0: TxDIS (default), 1: PRG_CNTL1.
3. Add bit 807Eh.2 to indicate the option of RxLOS or PRG_ALRM1, 0: RxLOS (default), 1: PRG_ALRM1.

Changes are made as follows (marked in yellow) to the following registers.

807E [2.2]	**1**	RO		**CFP and CFP2/4 Extended Identifier**		
			3	CFP4 Hardware TxDIS Pin (#11) Configuration	0: TxDIS, 1: PRG_CNTL1	0
			2	CFP4 Hardware RxLOS Pin (#12) Configuration	0: RxLOS, 1: PRG_ALRM1	0
			1~0	Reserved		0

A007	**1**			**PRG_CNTL1 Function Select**	**Selects, and assigns, a control function to PRG_CNTL1 (TX_DIS/PRG_CNTL for CFP4 module).**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: Assert/De-Assert of PRG_CNTL1 has no effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. 2~9: MSA reserved. 10: TX_DIS as default Init. Value* for CFP4 module. Note if host changes this value to other values, the hardware pin PRG_CNTL1	01h*

					may hold a state of either 1 or 0. This pin state may cause data traffic interruption, for example, if host change this register value from 10 to 1 the state of PRG_CNTL1 = 0 will cause an un-intended TRXIC reset. In order to avoid such situation host shall always write value 0 to this register and then set a correct PRG_CNTL1 to a desired state before a target value to this register. This approach shall be taken for all the in-fly reprogramming case and for A005h, and A006h. 11~255: Reserved.	

1

A00A	**1**			**PRG_ALRM1 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM1 (RX_LOS/PRG_ALRM for CFP4 module).**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10: RX_LOS as default Init. Value* for CFP4 module. No effect for other modules. 11~255: Reserved.	01h*

2

3 **3.4 Editor's Remark and Additional Proposal**

4 Code 10 should be reserved for registers B007h and B00Ah In the future.

4 ADDENDUM 4 ADDING MORE MODULE ID CODES TO REGISTER 8000H FOR OIF 4"X5" AND CFP2-ACO

4.1 Reference

Keywords	4x5 module ID number, CFP2-ACO
To CFP MSA MIS V2.2r06a	Register 8000h
To CFP MSA MIS Comment Log	Sumitomo 7, OIF 1

4.2 Problem Description

1. 4x5 module (Recently standardized in OIF) is not specified in 0x8000 "Module Identifier" Description.
2. Need a Module Identifier for OIF CFP2 ACO module

4.3 Solution

Make changes (marked in yellow) to the following registers.

8000	**1**	**RO**	**7~0**	**Module Identifier**	**00h: Unknown or unspecified, 01h: GBIC, * 02h: Module/connector soldered to motherboard,* 03h: SFP,* 04h: 300 pin XSBI, * 05h: XENPAK,* 06h: XFP,* 07h: XFF,* 08h: XFP-E,* 09h: XPAK,* 0Ah: X2,* 0Bh: DWDM-SFP,* 0Ch: QSFP, * 0Dh: QSFP+,* 0Eh: CFP, 0Fh: Reserved, (changed from CXP TBD) 10h: 168-pin 5"x7" MSA-100GLH, 11h: CFP2, 12h: CFP4, 13h: 168-pin 4"x5" MSA-100GLH, 14h: CFP2-ACO 15h ~ FFh : Reserved. Note values with "*" are copied from SFF8436, 8636, and 8024 for information only. CFP MSA MIS does not assign or control the IDs for these modules. Starting from value "0Eh", ID values overlap with those assigned by SFF documents. Based on the consultation with SFF 8024 Chairman it is deemed this overlap should not be an issue because SFF modules does not use MDIO as the management interface, they use I2C. Software which bases action on Identifier Values needs to recognize that synonyms exist and qualify the values by the management protocol.**	**N/A**

4.4 Editor's Remark and Additional Proposal

Note the text highlighted by yellow color.

5 ADDENDUM 5 ADDING MORE ETHERNET APPLICATION CODES TO REGISTER 8003H

5.1 Reference

Keywords	4x5 module ID number
To CFP MSA MIS V2.2r06a	Register 8003h
To CFP MSA MIS Comment Log	Sumitomo 7, Huawei 3

5.2 Problem Description

1. 10h of 0x8003 "Ethernet application code" is not clarified whether it is coherent or not (S7).
2. Register 8003 is lacking definitions for 40GE SMF 40 km 40GE-ER4, 40GE SMF 80 km 40GE ZR4, 100GE SMF 80 km 100G-ZR4 (H3).

5.3 Solution

Make changes (marked in yellow) to the following registers.

8003	**1**	**RO**	**7~0**	**Ethernet Application Code**	**Any CFP module which supports an application which includes Ethernet and additional applications such as SONET/SDH, OTN, Fibre Channel or other, shall record the value in Ethernet Application Code as follows.** **00h: Undefined type,** **01h: 100GE SMF 10km, 100GE-LR4,** **02h: 100GE SMF 40km, 100GE-ER4,** **03h: 100GE MMF 100GBASE-SR10,** **04h: 100GE MMF 100GBASE-SR4,** **05h: 40GE SMF 10km, 40GE-LR4,** **06h: 40GE SMF 40km, 40G-ER4,** **07h: 40GE MMF 40GBASE-SR4,** **08h: 40GE SMF 80km, 40GE-ZR4 (Non-standard),** **09h: 100GE SMF 80km, 100GE-ZR4 (Non-standard),** **0Dh: 40GE-CR4 Copper** **0Eh: 100GE-CR10 Copper,** **0Fh: 40G BASE-FR,** **10h: 100GE SMF 80km, 100GE-ZR1-Coherent** **11h: 100GE DWDM, 100GE-DWDM-Coherent** **12h~FFh: Reserved.**

5.4 Editor's Remark and Additional Proposal

The technology used for 40GE/100GE SMF 80 km is not clear at this moment. Coherent technology may be needed. Therefore code is assigned as requested but description marked as "Non-standard". MSA makes no implication regarding IEEE's standard decision.

6 ADDENDUM 6 ACRONYM CHANGE TO SOA AND VARIOUS DDM UNIT CHANGES DUE TO COHERENT TECHNOLOGY

6.1 Reference

Keywords	CFP MSA MIS V2.2r06a, SOA
To CFP MSA MIS V2.2r06a	SOA –Semi-conductor Optical Amplifier
To CFP MSA MIS Comment Log	Sumitomo 8-11

6.2 Problem Description

1. Name for acronym SOA is mentioned as “Solid-State Optical Amplifier" in Section 1.6 Glossary
2. Maximum monitor current range of 131.070 mA is too small for industry available SOA.

6.3 Solution

1. Make changes (marked in yellow) on page 14 of R06a

SOA	Semi-conductor Optical Amplifier

2. Make changes in the description column for the following registers:

8090	**2**	**RO**	**7~0**	**SOA Bias Current High Alarm Threshold**	**These threshold values are an unsigned 16-bit integer with LSB =2 uA by default, representing max value of 131.07 mA. For the case of coherent module (8003h = 02, 10 or 11) LSB = 8uA, representing max value of 524.280 mA. MSB stored at low address, LSB stored at high address.**	**2 uA**
8092	**2**	**RO**	**7~0**	**SOA Bias Current High Warning Threshold**		
8094	**2**	**RO**	**7~0**	**SOA Bias Current Low Warning Threshold**		
8096	**2**	**RO**	**7~0**	**SOA Bias Current Low Alarm Threshold**		

A031	**1**	**RO**	**15~0**	**SOA Bias Current A/D Value**	**These threshold values are an unsigned 16-bit integer with LSB =2 uA by default, representing 131.07 mA. For the case of coherent module (8003h = 02, 10 or 11) LSB = 8uA, representing a range of current from 0 to 524.280 mA. MSB stored at low address, LSB stored at high address.**	**0000h**

B031 [2.0]	**1**	**RO**	**15~0**	**SOA Bias Current A/D Value**	**These threshold values are an unsigned 16-bit integer with LSB =2 uA by default, representing 131.07 mA. For the case of coherent module (8003h = 02, 10 or 11) LSB = 8uA, representing a range of current from 0 to 524.280 mA. MSB stored at low address, LSB stored at high address.**	**0000h**

A2A0	**16**	**RO**	**15~0**	**Network Lane n Laser Bias Current monitor A/D value**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent. Measured laser bias current in uA, a 16-bit unsigned integer with LSB = 2 uA, representing a total measurement range of 0 to 131.072 mA. If Ethernet Application Code (8003h) is "-Coherent", then LSB is changed to 100uA. (Range is expanded to 0 ~ 6553.5 mA). Minimum accuracy shall be +/- 10% of the nominal value over temperature and voltage.**	**0000h**

6.4 Editor's Remark and Additional Proposal

JDSU has proposed to use a register bit field to store a scaling factor for these LSB units. However, there are multiple scaling factors needed so one won't be enough. The approach taken here is to put description in for each affected register to prompt vendor and user to scale the LSB unit corresponding to Module Identification number (8000h).

7 ADDENDUM 7 – DEFINING BITS FOR MODULE TO HOST SQUELCH ON LOL AND LOS

7.1 Reference

Keywords	Squelch, RX_LOL, RX_LOS
To CFP MSA MIS V2.2r06a	Page 103 A440h. Page 154 B640h
To CFP MSA MIS Comment Log	Juniper 15, JDSU 4, 5,Sumitomo 12,Oclaro 56

7.2 Problem Description

1. No register is defined to automatically enable or disable squelching RF output from module to host driven by RX_LOS and/or RX_LOL.
2. Need NVR register bits to indicate if automatic squelch feature is supported?
3. No register is defined to manually enable or disable squelching per host lane RX output (DUT output).

7.3 Solution

1. Use 8078h.7 to indicate if enable/disable squelch is supported.
2. Use A014h.9~8 to enable/disable automatic squelch driven by RX_LOS and RX_LOL respectively.
3. Add A040h for manual enable/disable squelch control on lane per bit base
4. Make similar changes to corresponding B-Page registers.
5. Detailed changes are marked in yellow as follows:

8078	**1**	**RO**		**Module Enhanced Options 2**		**N/A**
			7	Host Lane Output Squelch	0: Not supported, 1: Automatic/Manual Host lane Output squelch is supported.	N/A

A014	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RW	9	Automatic Host Lane Output Squelch on LOS (Optional)	0: Host Lane shall not squelch on RX_LOS. Host controls squelch using A040h 1: Host Lane shall squelch on RX_LOS (sync with A210h~A21Fh.4) per lane based.	0
		RW	8	Automatic Host Lane Output Squelch on LOL (Optional)	0: Host Lane shall squelch on RX_LOL. Host controls squelch using A040h. 1: Host Lane shall squelch on RX_LOL (sync with A210h~A21Fh.3) per lane based.	0

A040	**1**	**RW**	**All**	**Host Lane Output Squelch Control (Optional)**	**Each bit of this register controls corresponding host lane output squelch respectively. Note that toggling any bit in this register does not change module state. 0: Not squelch, 1: Squelch.**	**0000h**

1

B014 [2.0]	**1**			**Host Lane Control**	**This control acts upon all the host lanes.**	**0000h**
		RO	9	Automatic Host Lane TX Squelch on LOS (Optional)	0: Host Lane shall not squelch on RX_LOS. Host controls squelch using B040h, 1: Host Lane shall squelch on RX_LOS (sync with B200h~B20Fh.4) per lane based.	0
		RO	8	Automatic Host Lane TX Squelch on LOL (Optional)	0: Host Lane shall squelch on RX_LOL. Host controls squelch using B040h, 1: Host Lane shall squelch on RX_LOL (sync with B200h~B20Fh.3 or B600~B60Fh.0) per lane based.	0

2

B040	**1**	**RW**	**All**	**Host Lane Squelch Control (Optional)**	**Each bit of this register controls corresponding host lane output squelch respectively. Note that toggling any bit in this register does not change module state. 0: Not squelch, 1: Squelch.**	**0000h**
		RW	15~0	Host Lane n Squelch Control	Bits 15~0 squelches host lane 15~0 respectively. 0: No squelch, 1: Squelch.	0000h

3 ## 7.4 Editor's Remark and Additional Proposal

4 None.

8 ADDENDUM 8 – DEFINING BITS FOR MODULE TO NETWORK TX SQUELCH ON TX LOL (OPTIONAL)

8.1 Reference

Keywords	Network Lane Squelch, TX_LOL
To CFP MSA MIS V2.2r06a	
To CFP MSA MIS Comment Log	Oclaro 57

8.2 Problem Description

1. Need register to enable or disable squelching optical output signal from module on TX_LOL in network lanes.

8.3 Solution

1. Use 8078h.6 (Reserve) to indicate if Network Lane TX Squelch is supported.
2. Use reserved bit A011h.15 as “Automatic Network Lane TX Squelch Mode”. '0' Average Power is squelch on LOL. '1' OMA is squelch on LOL.
3. Use reserved bit A011h.4 as “Automatic Network Lane TX Squelch Control” to toggle between manual mode and automatic mode.
4. Add A041h for “Network Lane TX Squelch Control” per lane based.
5. Make similar changes to corresponding B-Page registers.
6. Please read RX as TX in bits 3-1 section below.

8078	**1**	**RO**		**Module Enhanced Options 2**		**N/A**
			6	Network Lane Output Squelch	0: Not supported, 1: Automatic/Manual Network lane TX squelch is supported.	N/A

A011	**1**			**Network Lane TX Control**	**This control acts upon all the network lanes.**	**0000h**
		RW	15	Automatic Network Lane TX Squelch Mode (Optional)	0: Network Lane shall squelch TX Average power on TX_LOL (sync with A210h~A21Fh.6) per lane base. 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with A210h~A21Fh.6) per lane base.	0
		RW	4	Automatic Network Lane TX Squelch Control (Optional)	0: Network lane automatic control on TX_LOL is off. Host controls each lane TX squelch using A041h. 1: Network lane automatic control on TX_LOL is on per lane base.	0

A041	**1**	**RW**	**All**	**Network Lane TX Squelch Control (Optional)**	**This control acts upon individual network lanes. Note that toggling any bit in this register does not change module state.**	**0000h**
		RW	15~0	Network Lane n TX Squelch (Optional)	Bits 15~0 squelches network lane 15~0 respectively. 0: No squelch, 1: Squelch.	0000h

B011	**1**			**Network Lane TX Control**	**This control acts upon all the network lanes.**	**0000h**
		RW	15	Automatic Network Lane TX Squelch Mode (Optional)	0: Network Lane shall squelch TX Average power on TX_LOL (sync with B1A0h~B1AFh.6) per lane base. 1: Network Lane shall squelch TX OMA power on TX_LOL (sync with B1A0h~B1AFh.6) per lane base.	0
		RW	4	Automatic Network Lane TX Squelch Control (Optional)	0: Network lane automatic control on TX_LOL is off. Host controls each lane output squelch using A041h. 1: Network lane automatic control on TX_LOL is on per lane base.	0

B041	**1**	**RW**	**All**	**Network Lane TX Squelch Control (Optional)**	**This control acts upon individual host lanes. Note that toggling any bit in this register does not change module state.**	**0000h**
		RW	15~0	Network Lane n TX Squelch (Optional)	Bits 15~0 squelches host lane 15~0 respectively. 0: No squelch, 1: Squelch.	0000h

8.4 Editor's Remark and Additional Proposal

None.

9 ADDENDUM 9 – ADD DIVIDER OF 1/8 TO RECEIVER MONITOR CLOCK OPTIONS REGISTER 807Ah

9.1 Reference

Keywords	MCLK Divisor of 1/8, Receiver Monitor Clock Options
To CFP MSA MIS V2.2r06a	Register 807Ah.
To CFP MSA MIS Comment Log	FOC 7.

9.2 Problem Description

1. Comment on MIS_V2p_r04, Sumitomo suggested that "It seems that 1/8 for CFP2 4x25G option and CFP4 (TX MCLK Option 2) and 1/160 for CFP4 (TX MCLK Option 5) are missing. And add them to 8079h and 807Ah" in #6 and Editor's response are "Added in V2.2r05b." However 1/8 for CFP2 4x25G are added only in 8079h on 2.2 r06a.

9.3 Solution

1. Add 1/8 for CFP2 4x25G option in 807Ah. Change is marked as yellow color.

807A	**1**	**RO**		**Receiver Monitor Clock Options**	**The CFP module may supply an optional receiver monitor clock. This clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a faction of either host lane rate or a network lane rate. A module may support multiple options. For the below bit values, 0 = not supported, 1 = supported.**			**0**
					CFP or CFP2 10x10 mode	CFP2 4x25 mode or CFP4	Of Source Lane	
			7	RX MCLK Option 7	1/16	1/40	Host	0
			6	RX MCLK Option 6	1/16		Network	0
			5	RX MCLK Option 5	1/64	1/160	Host	0
			4	RX MCLK Option 4	1/64	-	Network	0
			3	Reserved	-	-	Host	0
			2	RX MCLK Option 2	1/8	1/8	Network	0
			1	RX MCLK Option 1	-	1/32	Host	0
			0	RX MCLK Option Support	Indicating whether this option is supported or not. 0=not supported, 1=Supported.			0

9.4 Editor's Remark and Additional Proposal

None.

10 ADDENDUM 10 – FIRMWARE FIELD UPGRADE FILE FORMAT

10.1 Reference

Keywords	Firmware field upgrade, firmware file format
To CFP MSA MIS V2.2r06a	Section 4.12.5, Table 21
To CFP MSA MIS Comment Log	Oclaro 56

10.2 Problem Description

Firmware download file format is not defined.

10.3 Solution

Add the following verbiage to Description of Command “Download Image Block” in Table 21 on page 62/158, as highlighted in color yellow.

00h	21h	0021h	Download Image Block	L	Y	Host to download a block of software image to module. PL0 = Image Block Number (max 65535). The rest of CDB Payload is the software image block which can contain additional descriptor per vendor design. Note total image size is limited to 1019 x 65536 = 66.78 MB. Expected CMD specific Reply: 0140h: Image download successful. PL0 = Block number just downloaded. 0340h: CRC image block CRC error. PL0 = Block number just downloaded. CFP MSA MIS shall not specify a specific file format leaving it as vendor specific. It is recommended to use file extensions such as .asc or .bin to signify ASCII or binary coded file. Note that the 16-bit payload data shall use big endian.
CDB Command Class 1 – Register Access						

10.4 Editor’s Remark and Additional Proposal

No need to define file format because the file format is made by each vendor. Any bootloader in vendor's firmware shall know what the format is.

--- End of Document Addendums to CFP MSA MIS V2.2r06a Ver.1.0r1 ---