

Study of High Speed TX& RX Pin Separation in Pluggable Modules

CFP MSA Member Companies:

Avago Technologies

Finisar Corp.

Fujitsu Optical Components

Opnext, Inc.

Sumitomo Electric Industries

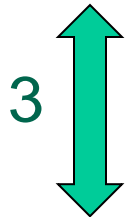
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Existing Module Pin Allocation

XAUI

60	GND
59	TX LANE1-
58	TX LANE1+
57	GND
56	TX LANE0-
55	TX LANE0+
54	GND
53	GND
52	GND
51	RX LANE3-
50	RX LANE3+
49	GND
48	RX LANE2-
47	RX LANE2+
46	GND



XFP

16	GND
17	RD-
18	RD+
19	GND
20	VCC2
21	P_Down/R
22	VCC2
23	GND
24	REFCLK+
25	REFCLK-
26	GND
27	GND
28	TD-
29	TD+
30	GND



SFP+

11	VEER
12	RD-
13	RD+
14	VEER
15	VccR
16	VccT
17	VEET
18	TD+
19	TD-
20	VEET



TX ↔ RX pin separation

Existing Module Pin Allocation

CFP

124	GND
123	TX3n
122	TX3p
121	GND
120	TX2n
119	TX2p
118	GND
117	TX1n
116	TX1p
115	GND
114	TX0n
113	TX0p
112	GND
111	GND
110	N.C.
109	N.C.
108	GND
107	RX9n
106	RX9p
105	GND
104	RX8n
103	RX8p
102	GND
101	RX7n
100	RX7p
99	GND
98	RX6n



QSFP+

38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMMode
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	RX4p
24	Rx4n
23	GND
22	RX2p
21	RX2n
20	GND

Module Card Edge

	GND	1
	TX2n	2
	TX2p	3
	GND	4
	TX4n	5
	TX4p	6
	GND	7
	ModseL	8
	ResetL	9
	VccRx	10
	SCL	11
	SDA	12
	GND	13
	RX3p	14
	Rx3n	15
	GND	16
	RX1p	17
	RX1n	18
	GND	19



TX ↔ RX pin separation

CFP4 Pin Allocation Alternatives

CFP4 Baseline

CFP4	
Top Row	
56	GND
55	TX3n
54	TX3p
53	GND
52	TX2n
51	TX2p
50	GND
49	TX1n
48	TX1p
47	GND
46	TX0n
45	TX0p
44	GND
43	(REFCLKn)
42	(REFCLKp)
41	GND
40	RX3n
39	RX3p
38	GND
37	RX2n
36	RX2p
35	GND
34	RX1n
33	RX1p
32	GND
31	RX0n
30	RX0p
29	GND



CFP4 with less pins

CFP4	
Top Row	
50	GND
49	TX3n
48	TX3p
47	GND
46	TX2n
45	TX2p
44	GND
43	TX1n
42	TX1p
41	GND
40	TX0n
39	TX0p
38	GND
37	RX3n
36	RX3p
35	GND
34	RX2n
33	RX2p
32	GND
31	RX1n
30	RX1p
29	GND
28	RX0n
27	RX0p
26	GND



TX ↔ RX pin separation

CFP4 REFCLK Pin Use

❑ Un-retimed applications

By definition, the module does not use REFCLK in these applications. These are also the most cross-talk sensitive applications because they have large channel loss, for example 30dB to 40dB for passive CU, or stringent jitter specifications for example linear MMF RX output. Since the module does not use REFCLK, the REFCLK pins can be internally grounded for maximum TX and RX isolation.

❑ Retimed applications

Applications that use REFCLK, i.e. re-timed, have moderate channel loss, for example 10dB in CEI-28G VSR. Therefore adjacent interferers have similar signal strength. Further, the stronger signal is RX and the weaker signal is REFCLK, which is much less of an issue because REFCLK is narrow band filtered.

❑ Conclusion

9 high speed differential pairs is the minimum number of pins for the CFP4 top row to maintain good cross-talk performance for all applications. This results in 56 total module pins.