Contribution Number: oif2011.214.03

Working Group:	**PLL**
Title:	**MLG (Multi-Link Gearbox) Project Start Proposal**
Meeting:	**Q3 2011**
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Abstract: 10:4 Mux Gearbox is used to convert a single 100Gb/s link striped across 10 lanes into 4x25G lanes, and a 4:10 DeMux Gearbox is used to convert the 4x25G lanes back to a single 100Gb/s link striped across 10 lanes. The MLG (Multi-Link Gearbox) Project will define 10:4 Mux MLG function to convert multiple (up to 10) independent 10Gb/s links into 4x25G lanes, and a 4:10 DeMux MLG function to convert the 4x25G lanes back to multiple (up to 10) independent 10Gb/s links.

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MLG (Multi-Link Gearbox) Project Proposal

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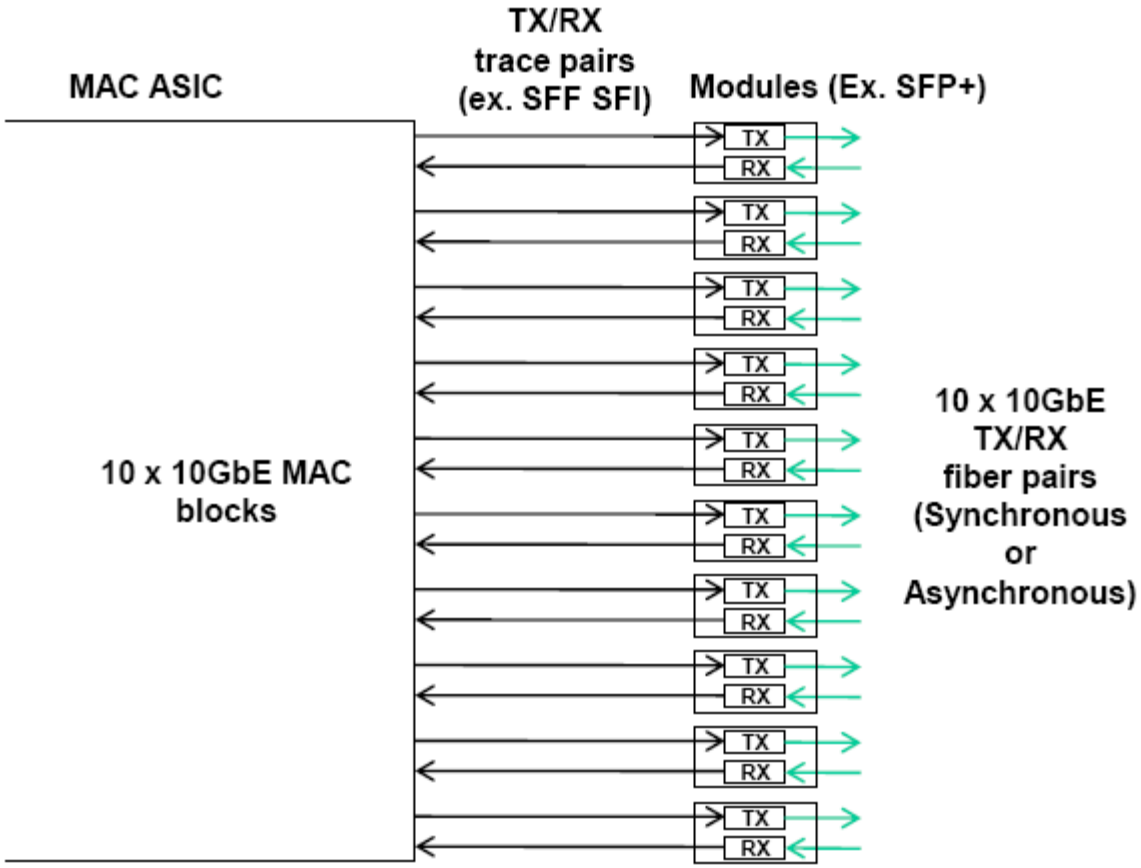
Existing 10GBASE-R Port Application



- Switch ASIC 10G I/O connects directly to module 10G I/O
- Some applications require separate 10G re-timers behind 10G modules

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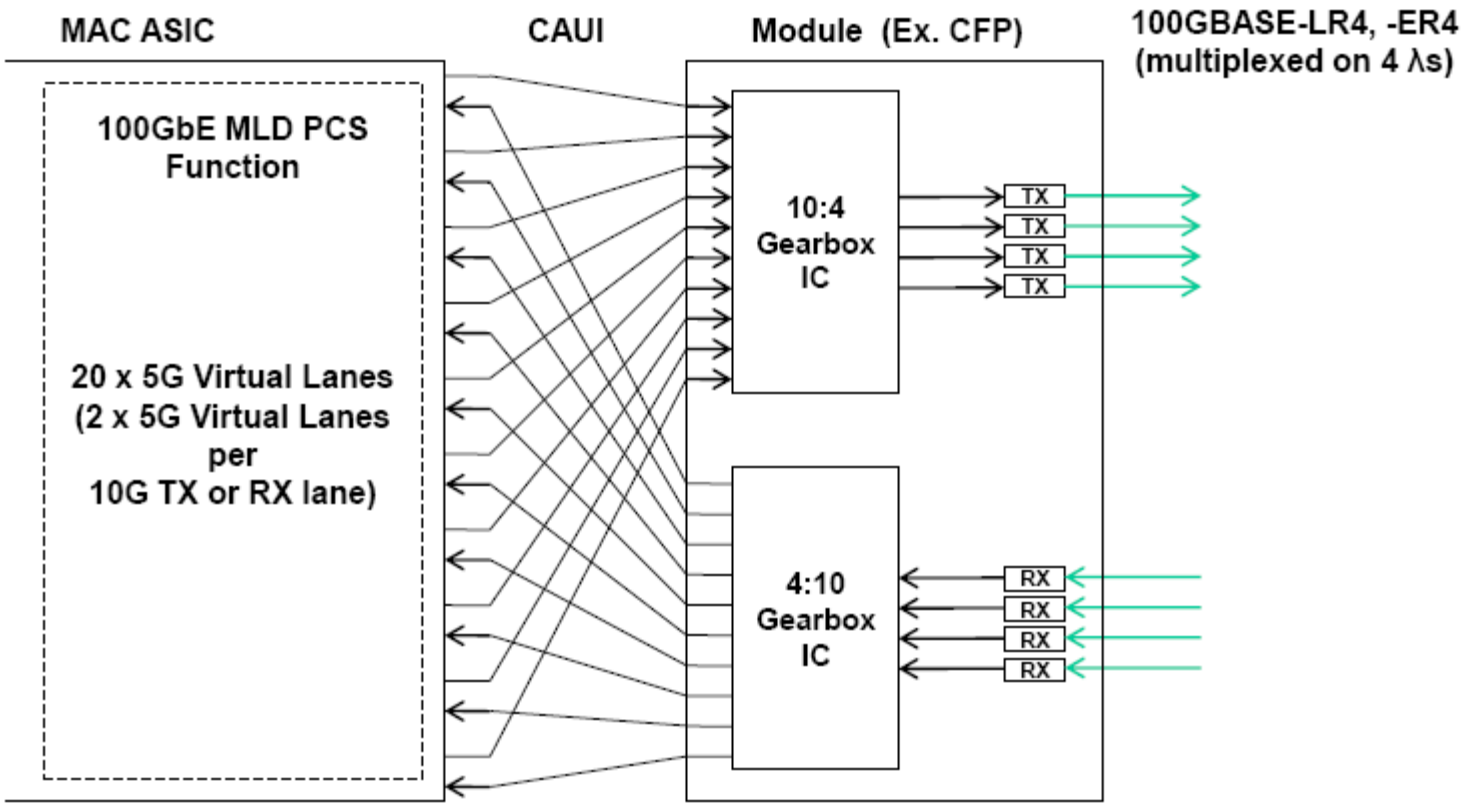
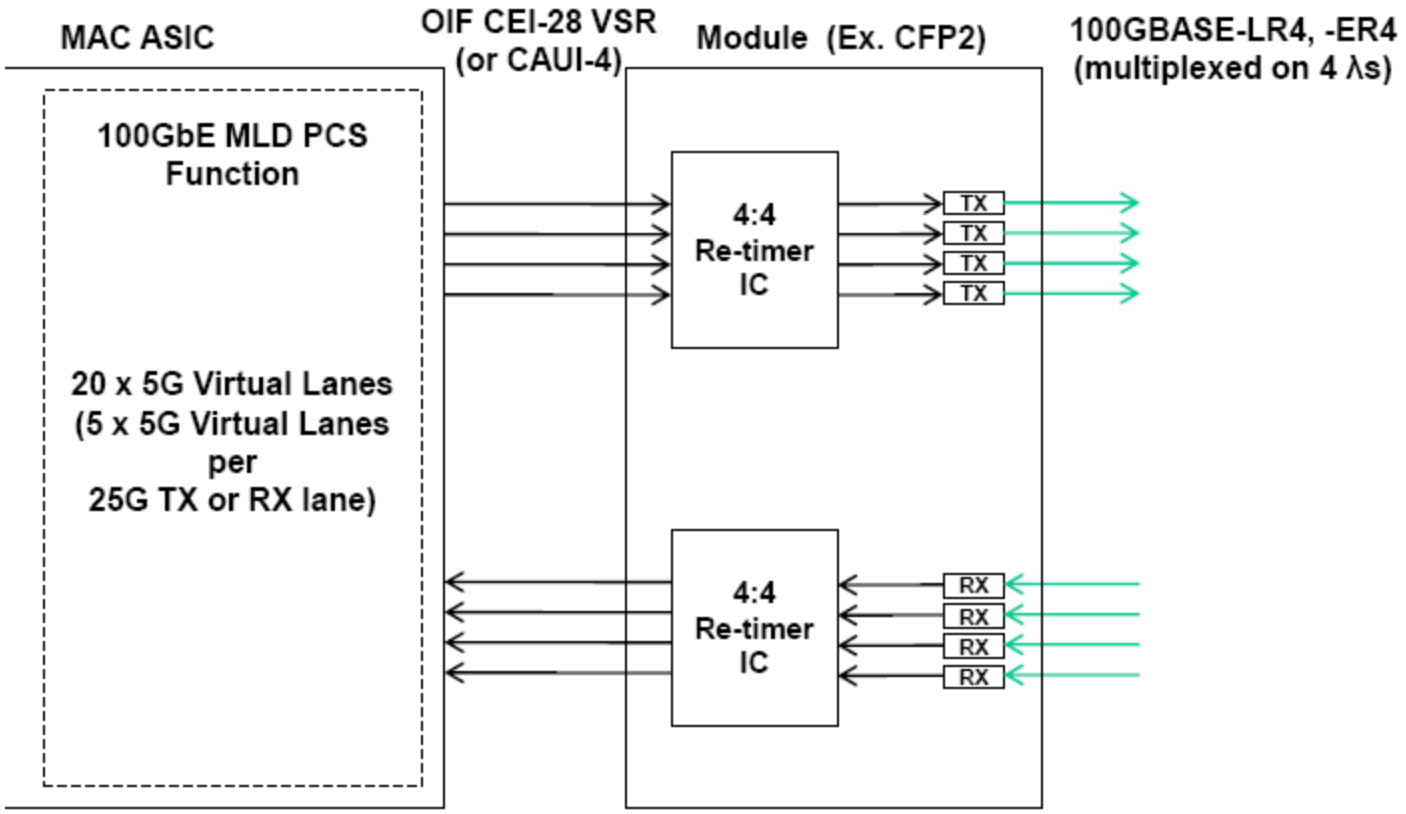
Existing 10:4 Gearbox IC Application



- Existing 10:4 Gearbox ICs do not preserve 10G physical lanes and do not support independent 10G lanes (desirable for some apps.)
- MLD PCS layer in the MAC ASIC re-assembles 100GbE bit stream
- MLD PCS supports only one link

Future 25G I/O Application



- Switch ASIC 25G I/O connects directly to module 25G I/O
- MLD PCS layer in the MAC ASIC is required to re-assemble 100GbE bit stream
- MLD PCS supports only one link

OIF OPTICAL INTERNETWORKING FORUM

Project Start Justification 1

- Project name
  - MLG (Multi-Link Gearbox)
- Problem statement
  - Back to back 10:4 Gearbox ICs do not preserve 10G physical lane structure. This limits their application to support only a single 100Gb/s link. They can not support independent 10G links.
- Scope
  - MLG Project will define in-band coding that preserves 10GBASE-R physical lane-to-lane ordering and in-lane bit ordering to support synchronous and asynchronous 10G lanes
  - MLG definition will require manual Gearbox mode configuration
  - MLG Project will not define coding for any other 10G lanes, including 10GBASE-KR, 10GBASE-W, STM-64, OTU2, or OTU2e
  - MLG Project will not define electrical specifications
  - MLG Project will not define optical specifications
  - MLG Project will not define Auto Negotiation
- Objective
  - Preserve 10GBASE-R specification compliance after a MLG to MLG link

Project Start Justification 2

- Output
  - Single IA that supports 10GBASE-R 10G lanes (except -KR)
  - Extension to additional applications may result in future IAs, supporting other 10G lane types, for example:
    - Independent 10GBASE-W, STM-64, OTU2, or OTU2e lanes
    - Independent 40GBASE-R or OTL3.4 4x10G lane groupings
- Requirements
  - Preserve 25.78125Gb/s lane rate to enable carrying 10G lanes across 4x25G links such as 100GBASE-LR4 or 100GBASE-ER4
  - Meet 802.3ba Gearbox to Gearbox skew spec between MLGs
  - Do not affect operating lanes by failure or turn-on of any 10G lane
  - Support 10GBASE-R lanes formatted per 802.3 Clauses 49 & 51
- Benefits to OIF
  - MLG enables support of new Gearbox applications including:
    - 10GBASE-R virtual link
    - 10GBASE-R electrical port expander
    - 10GBASE-R optical port expander

OIF OPTICAL INTERNETWORKING FORUM

Project Start Justification 3

- Relationships with other OIF working groups
  - MLG Project will be contained within the PLL
- Relationships with other industry groups
  - MLG Project will leverage the IEEE 802.3ba CAUI and PCS, and ITU-T G.709 OTL4.4 and Appendix X OTL4.10 standards
  - MLG Project will liaison with IEEE 802.3
- Proposed Timeline
  - Q3'11: Project Start
  - Q4'11: Last New Proposals
  - Q1'12: Select Technical Approach & Adopt Baseline Text
  - Q2'12: Straw Ballot
  - Q3'12: 2nd Straw Ballot
  - Q4'12: Principal Member Ballot

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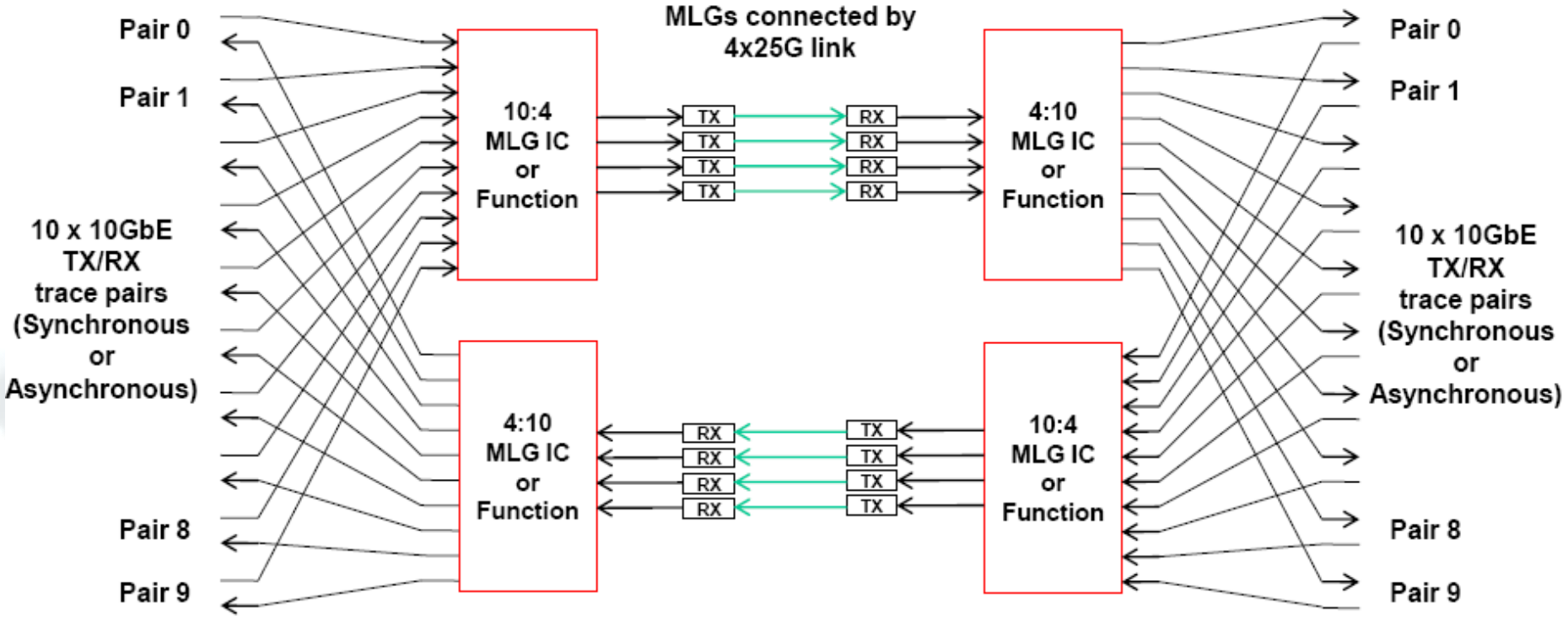
10GBASE-R Virtual Link



- MLG adds new Mux and DeMux functionality to existing Gearbox
- MLG enables ten 10GBASE-R links to be carried across a 4x25G link
- MLG preserves 10G physical lane structure ordering and timing without a 100GbE MAC or OTU4 Framer
- Supported in 1st MLG IA (except -KR)

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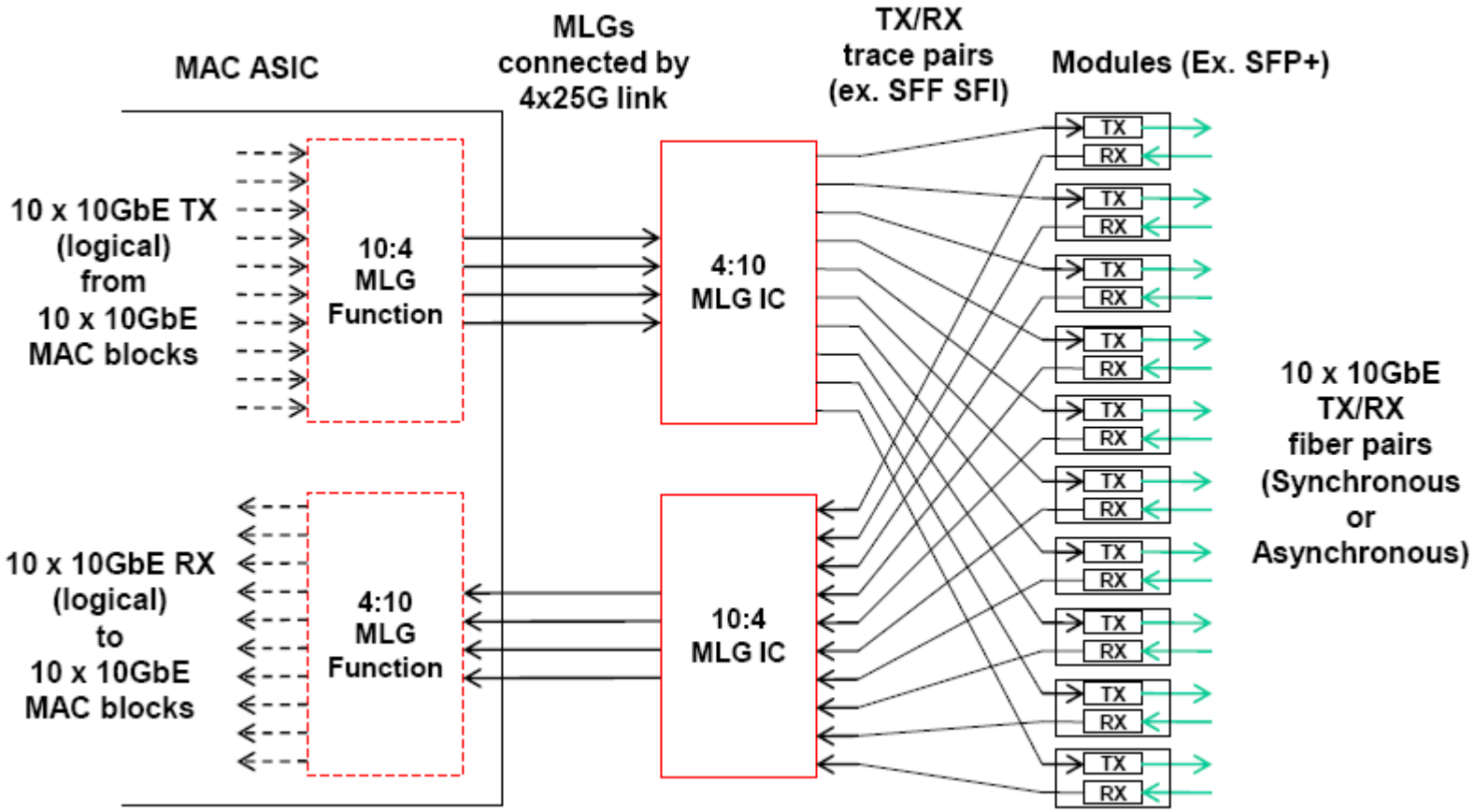
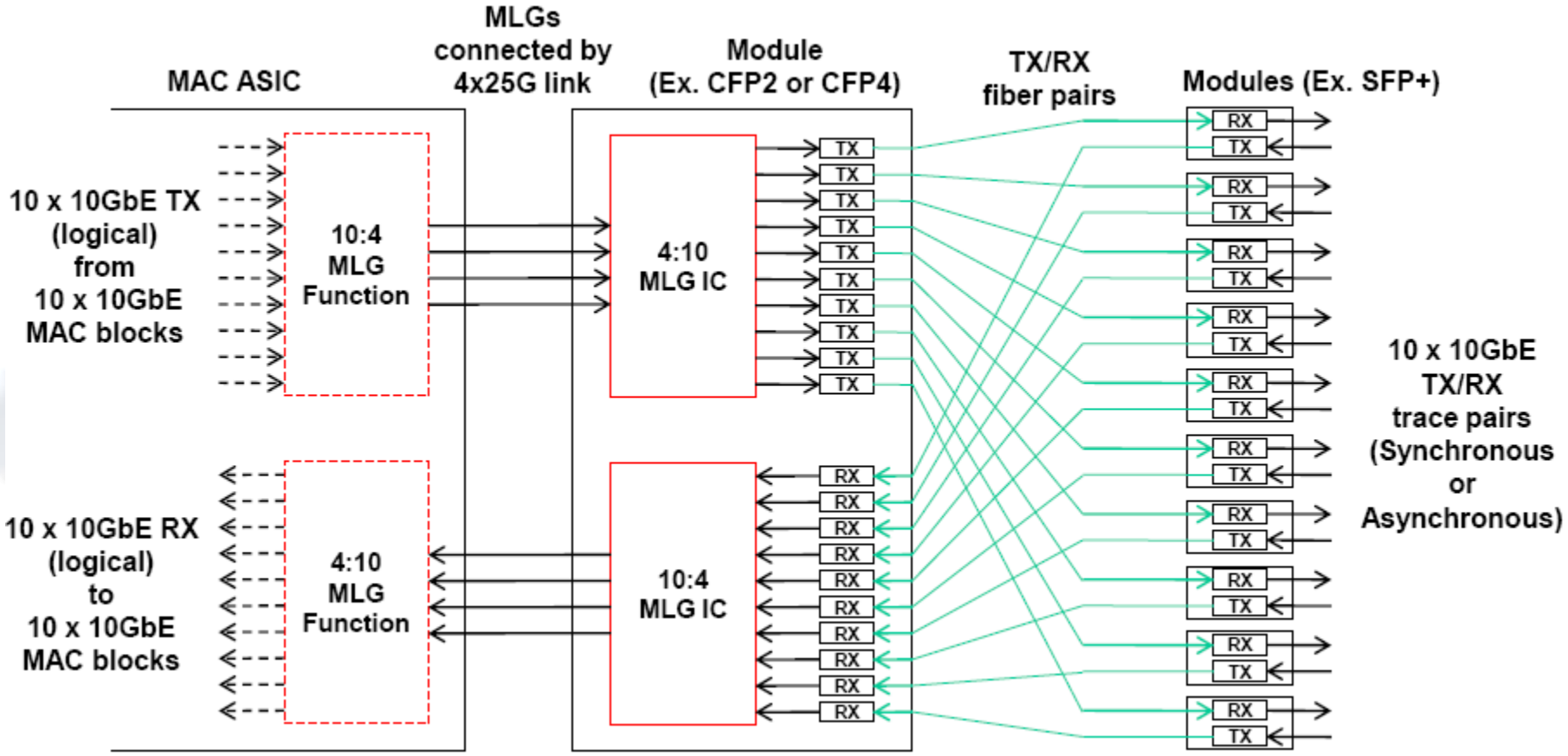
Electrical 10GBASE-R Port Expander



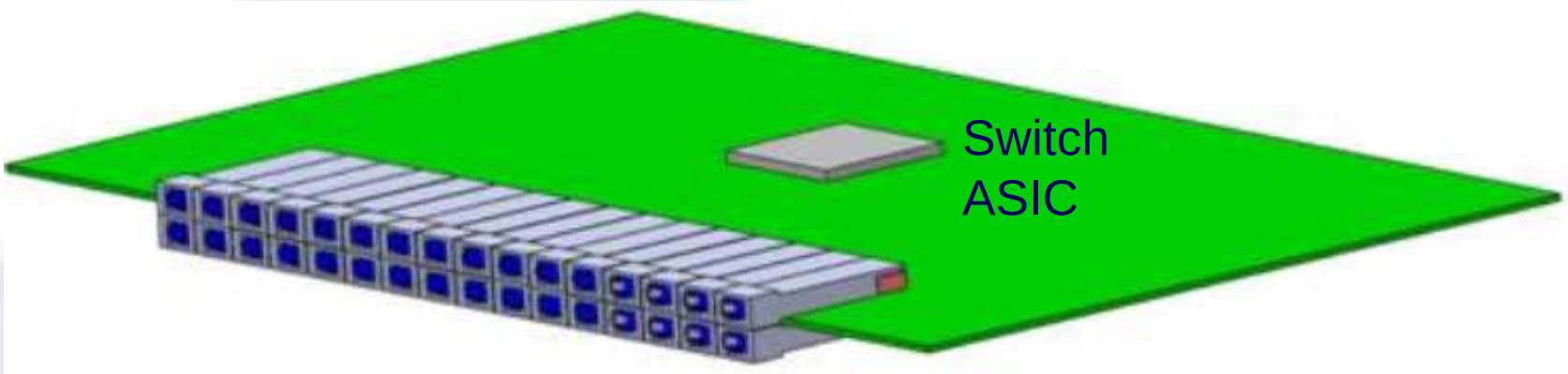
- 10G I/O limits Switch ASICs to ~128 10GbE ports
- 25G I/O limited Switch ASICs can support ~320 10GBASE-R ports

Optical 10GBASE-R Port Expander



- 10G I/O limits Switch ASICs to ~128 10GbE ports
- 25G I/O limited Switch ASICs can support ~320 10GBASE-R ports

Optical 10GBASE-R Port Expander Example



Host card

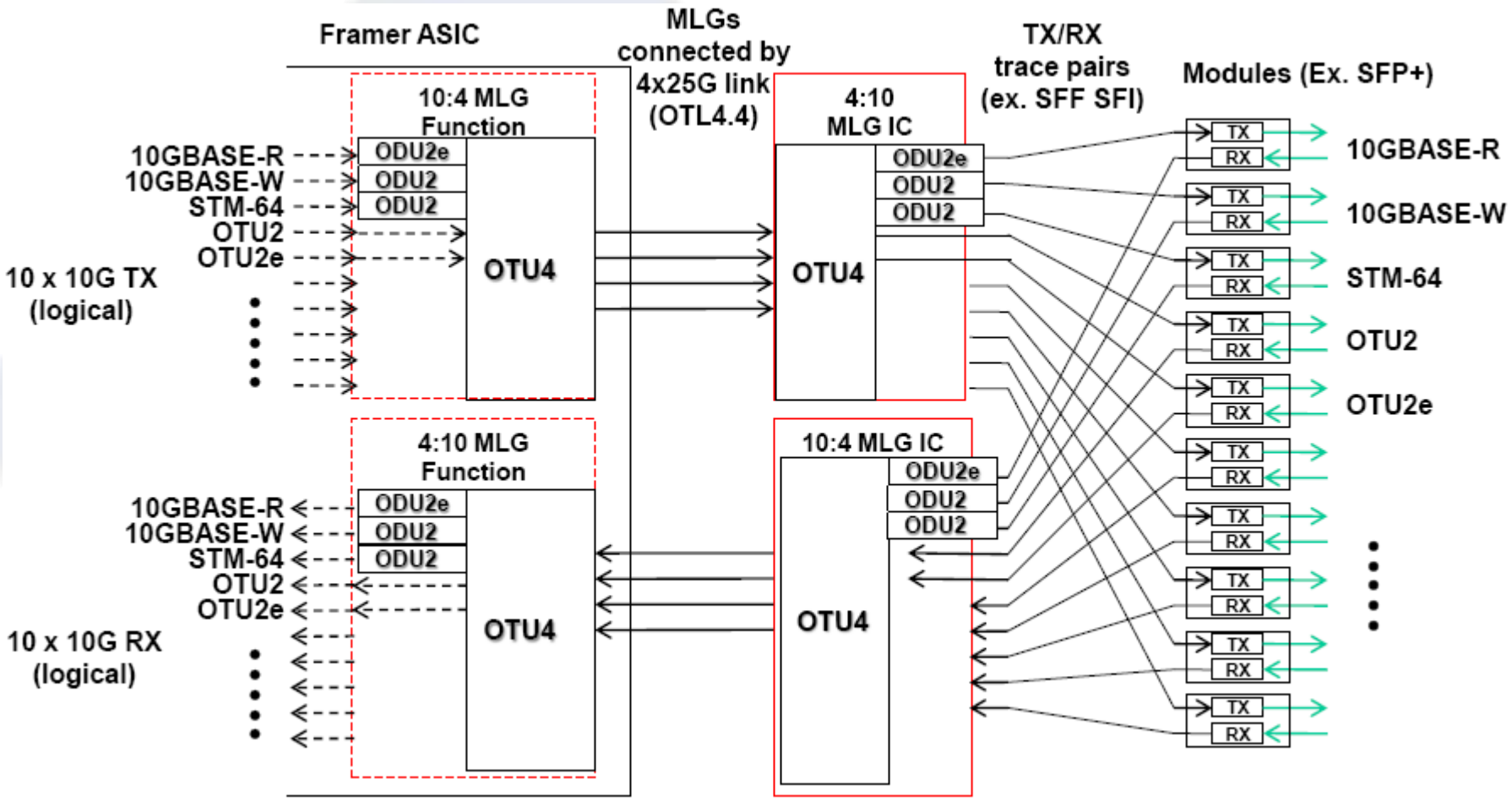
- 1 U.I. card pitch
- 1 Switch ASIC with 128 x 25G I/O
- 32 CFP4s each with 4:10 MLG IC, 10x10G array optics, and 24MTP MMF connector

Supported links

- 32 100GBASE-SR10 parallel MMF
- 320 “10GBASE-SR” duplex MMF

OIF OPTICAL INTERNETWORKING FORUM

All-purpose 10G Port Expander



- OTN mapping enables heterogeneous combination of 10G port types with independent timing (except -KR)
- Not defined in 1st MLG IA