CFP MSA Hardware Specification

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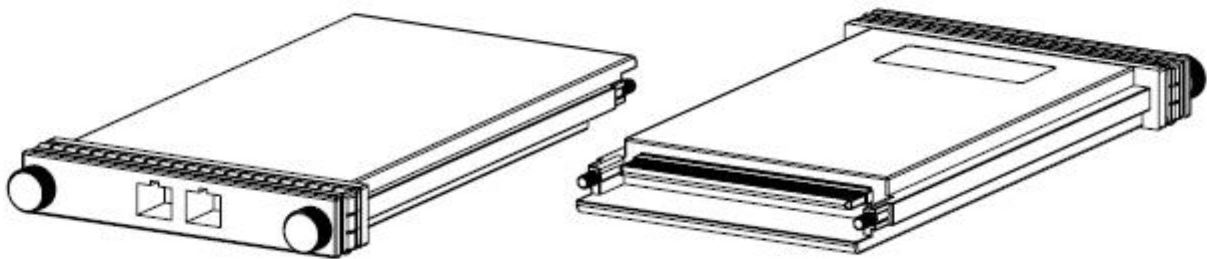

Description:

This Multi-Source Agreement (MSA) defines the form factor of an optical transceiver to support 40Gbit/s and 100Gbit/s interfaces for Ethernet, Telecommunication and other applications. The members of the MSA have authored this document to provide an industry standard form factor for new and emerging high speed communications interfaces.

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REVISION HISTORY

Draft	Date	Revised Items
External NDA Draft 0.2	14 Aug. 2008	
External NDA Draft 0.3	29 Aug. 2008	• Corrected Figure 10 in Draft 0.2 which showed wrong pin orientation – now figure 4-8; • Clarified ambiguity in Pin & Soft mode descriptions; • Updated Pin Map (non-traffic portion only) • Changed RX_RCLK to RX_MCLK

External NDA Draft 0.4	26 Nov. 2008	• MDIO management interface chosen – I2C will not be supported
		• Added Topics Under Review Table
		• Added Control & Alarm Pin Descriptions
		• Module Dimensions:
		  • Length: Module lengthened to allow for EMI finger attachment
		  • Height: Module height closed at 13.6mm
		  • Width: Modified for rail design
		• Updated References
		• Updated Pin Map to 148pins – extra signal grounds

Publication	March 23 2009	• Revised Control & Alarm Pin Descriptions & Electrical specifications • Added Power supply requirements • Host Mechanicals updated • Module Drawings updated • Updated Figures & Timing Diagrams • Updated Pin Map Control Pin locations
Publication; Rev 1.4	June 7, 2010	• Welcomed Avago Technologies to the CFP MSA • Reference Clock Characteristics detailed • Updated Mechanical Drawings • Updated LC connector orientation with figure • Added pointer to external Mechanical Drawing • Populated timing requirements in Table 2-7 • Refined figures 2-1 & 2.-4 • Updated Pin-Map to reflect new naming conventions for Programmable Alarm functions & corrected typos • Removed SFI-S and SFI-5.2 and replaced with OTL/STL • Updated pin-map to remove Deskew lanes required by SFI-S and SFI-5.2 • Updated 40GE serial nomenclature to reflect 40GBASE-FR • Updated references

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REFERENCE DOCUMENT

[1] IEEE P802.3ba
[2] XLAUI / CAUI
[3] Optical connector; TBD
[4] Electrical connector; TBD
[5] CFP MSA Management Interface Specification 1.4
[6] JEDEC Standard JESD8C.01, Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits
[7] JEDEC Standard JESD8-12A.01, 1.2 V +/- 0.1V (Normal Range) and 0.8 - 1.3 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits
[8] IEEE 802.3 Clause 45 MDIO
[9] ITU-T RECOMMENDATION G.709, Amendment 3
[10] NEBS Requirements: Physical Protection; Document Number GR-63
[11] GR-1221-CORE (Generic Reliability Assurance Requirements for Passive Optical Components)

1 GENERAL

1.1 SCOPE

This Multi-Source Agreement (MSA) defines the form factor of an optical transceiver which can support 40Gbit/s and 100Gbit/s interfaces for Ethernet, Telecommunications and other applications. The electrical interface will vary by application, but the nominal signaling lane rate is 10Gbit/s per lane and documentation is provided for CAUI, XLAUI, OTL4.10, OTL3.4, and STL256.4 electrical interface specifications. The CFP module may be used to support single mode and multimode fiber optics.

The CFP modules and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module.

CFP MSA is an acronym for 100G[1] Form factor Pluggable Multi-Source Agreement.

1.1.1 Application & Qualification

All optoelectronic devices used within CFP MSA modules shall meet the reliability requirements as specified per Telcordia GR-468-CORE (Generic Reliability Assurance Requirements for Optoelectronic Devices Used in Telecommunications Equipment) or if necessary GR-1221-CORE (Generic Reliability Assurance Requirements for Passive Optical Components).

In addition, the CFP MSA modules are intended for use in equipment qualified per Telcordia GR-63-CORE Network Equipment-Building System (NEBS) Requirements for Physical Protection.

1.2 CFP BLOCK DIAGRAM

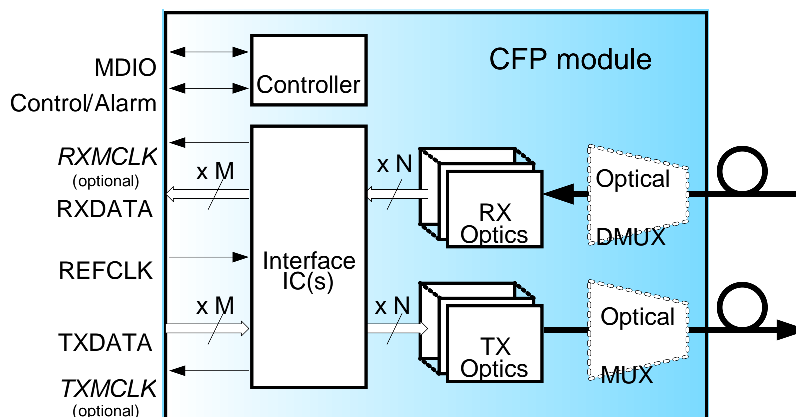

Figure 1-1: CFP Block Diagram

[1] C = 100 in Roman numerals; Centum

1.3 FUNCTIONAL DESCRIPTION

The CFP module is a hot pluggable form factor designed for optical networking applications. The module size has been chosen to accommodate a wide range of power dissipations and applications. The module electrical interface has been generically specified to allow for vendor specific customization around various "M" lane by 10Gbit/s interfaces.

1.3.1 Hot Pluggable

A CFP module is defined to be hot pluggable. Hot Pluggable is defined as permitting module plugging and unplugging with Vcc applied, with no module damage and predictable module behavior as per the State Transition Diagram. As shown in Figure 5-9: Pin Map Connector Engagement, the Module Absent (MOD_ABS) pin and Module Low Power (MOD_LOPWR) pin are physically guaranteed to be the last pins to mate. Please refer to the state diagram in the "CFP MSA Management Interface Specification", or alternately a reference version is shown at Figure 2-9: CFP MSA Start-Up Flow Diagram for detailed functional description.

2 CFP Hardware Signaling Pins

The control and status reporting functions between a host and a CFP module use non-data signal pins on the 148-pin connector. The signal pins work together with MDIO interface to form a complete HOST/CFP management interface. The signal pins provide status reporting. There are 6 Hardware Control pins, 5 Hardware Alarm pins, and 8 pins dedicated to the MDIO interface.

2.1 Hardware Control Pins

The CFP Module supports real-time control functions via hardware pins, listed in Table 2-1: Control Pins.

Table 2-1: Control Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
30	PRG_CNTL1	Programmable Control 1 *MSA Default: TRXIC_RSTn, TX & RX ICs reset,* *"0": reset, "1"or NC: enabled*	I	3.3V LVCMOS	per CFP MSA Management Interface Specification [5]		Pull – Up[2]
31	PRG_CNTL2	Programmable Control 2 *MSA Default: Hardware Interlock LSB*	I	3.3V LVCMOS			Pull – Up[2]
32	PRG_CNTL3	Programmable Control 3 *MSA Default: Hardware Interlock MSB*	I	3.3V LVCMOS			Pull – Up[2]
36	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull – Up[2]
37	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[2]
39	MOD_RSTn	Module Reset (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[3]

2.2 Hardware Control Pins: Functional Description

2.2.1 Programmable Controls (PRG_CNTLs)

These control pins allow for the system to program certain controls via a Hardware pin. The default setting for Control 1 is control of the Transmit & Receive Reset. The default setting for the Controls 2 and 3 are the Hardware Interlock described in section 2.2.1.4. The electrical signaling requirements are specified in Table 2-5.

2.2.1.1 Programmable Control 1 Pin

Programmable Control Pin 1 (PRG_CNTL1) is an input pin from the Host, operating with programmable logic. It is pulled up in the CFP module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any steady state except Reset. The CFP MSA specifies that the default function be Transmit & Receive circuitry reset (*TRXIC_RSTn*) with active-low logic. When TRXIC_RSTn is asserted (driven low) the digital transmit and receive circuitry is reset clearing all FIFOs and/or resetting all CDRs and/or DLLs. When de-asserted, the digital transmit and receive circuitry resumes normal operation.

2.2.1.2 Programmable Control 2 Pin

Programmable Control Pin 2 (PRG_CNTL2) is an input pin from the Host, operating with programmable logic. It is pulled up in the CFP module. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any state except Reset or Initialize. The CFP MSA specifies that the default function be the least significant bit of a two-bit code for Hardware Interlock.

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[2] Pull-Up resistor (4.7kOhm to 10 kOhm) is located within the CFP module.

[3] Pull-Down resistor (4.7kOhm to 10 kOhm) is located within the CFP module

2.2.1.3 *Programmable Control 3 Pin*

Programmable Control Pin 3 (PRG_CNTL3) is an input pin from the Host, operating with programmable logic. It is pulled up in the CFP. It can be re-programmed over MDIO registers to another MDIO control register while the module is in any state except Reset or Initialize. The CFP MSA specifies that the default function be the most significant bit of a two-bit Code for Module Power Class rating. Together with the Programmable Control Pin 2, the host uses this Code as the Hardware Interlock to inform what the power rating is supported by host at the connector. The Code is listed in Table 2-2.

2.2.1.4 *Hardware Interlock*

The CFP MSA encompasses a wide range of applications and thus the expected power consumption of the CFP module will vary accordingly. Often systems are limited in the amount of power which can be dissipated in various module slots. The Hardware Interlock provides for four different power consumption levels. The module shall compare the maximum power dissipation under vendor specified operating conditions to the host system cooling capacity value communicated via the Hardware Interlock. See the Table 2-2: Hardware Interlock for definition of the Hardware Interlock function.

The Hardware Interlock pins shall be kept at a static value during the transient Initialize state, and any change to the values will result in unpredictable module behavior.

The default functions of Programmable Control Pin 2 (PRG_CNTL2) and Programmable Control Pin 3 (PRG_CNTL3) are to define the LSB and MSB of Hardware Interlock. The host uses this Code as the Hardware Interlock to inform what the power rating is supported. If the CFP Module Power Dissipation exceeds the power rating of the host system as communicated by the Hardware Interlock, the module is placed in low power state. This low power state is the same as the state of the module if MOD_LOPWR hardware pin is asserted, see section 2.2.3. Note that setting the two Hardware Interlock bits to “11” (or N.C.) is equivalent to Hardware Interlock being unused; the module will not go into low power mode.

Table 2-2: Module Power Classes defined by Hardware Interlock

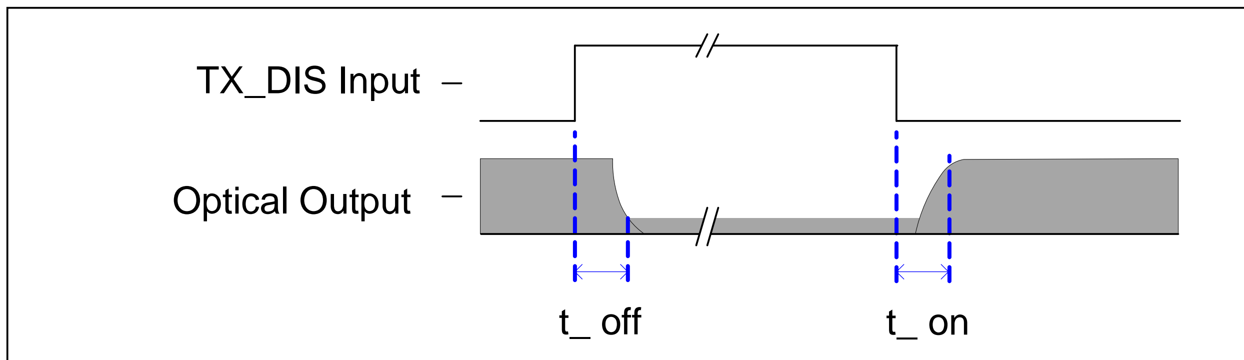
Hardware Interlock Description		CFP Module Power Dissipation	Power Class
MSB	LSB		
0	0	≤ 8 W	1
0	1	≤ 16 W	2
1	0	≤ 24 W	3
1	1	≤ 32 W	4

2.2.2 *TX Disable Pin*

TX Disable Pin (TX_DIS) is an input pin from the Host, operating with active-high logic. This pin is pulled up in the CFP. When TX_DIS is asserted, all of the optical outputs inside a CFP module shall be turned off. When this pin is de-asserted, transmitters in a CFP module shall be turned on according to a predefined TX turned-on process which is defined by the state diagram shown in the “CFP MSA Management Interface Specification”. A maximum time is defined for the transmitter turn-on process. This time is vendor and/or

technology specific and the value is stored in a MDIO register. See the "CFP MSA Management Interface Specification" for more details.

Figure 2-1: Tx Disable Timing Diagram



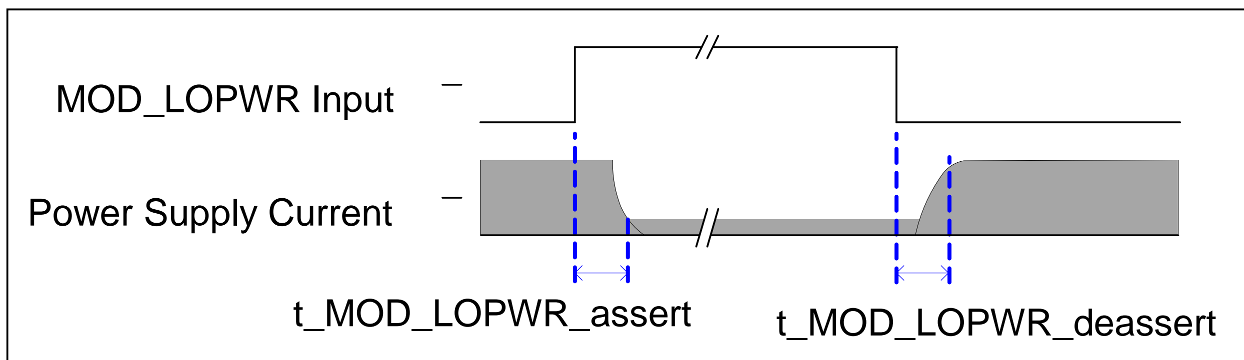
2.2.3 Module Low Power Pin

Module Low Power Pin (MOD_LOPWR) is an input pin from the host, operating with active-high logic. It is pulled up in the CFP. When MOD_LOPWR is asserted the CFP module shall be in the Low-Power State and will stay in the Low Power State as long as it is asserted. When de-asserted, the CFP shall initiate the Full-Power-up process. This pin on the CFP module is 1 mm shorter than the Vcc power supply pins. This design helps to control the inrush and turn-off current during module plug-in (insertion) and pull-out (extraction).

In Low Power mode the module can communicate via the MDIO management interface. While the module is in low power mode it has a maximum power consumption of <2W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

A maximum time is defined for the High-Power-up process, and a MDIO register is specified in the "CFP MSA Management Interface Specification".

Figure 2-2: Module Low Power Timing Diagram



2.2.4 Module Reset Pin

Module Reset Pin (MOD_RSTn) is an input pin from the Host, operating with active-low logic. This pin is pulled down in the CFP with a pull-down resistor value of 4.7kOhm to 10 kOhm. When MOD_RSTn is asserted (driven low) the CFP module enters the Reset State. When de-asserted, the CFP module comes out of the Reset State and shall begin an initialization process as part of the overall module startup sequence.

2.3 Hardware Alarm Pins

The CFP Module supports alarm hardware pins, listed in Table 2-3: Hardware Alarm Pins.

Table 2-3: Hardware Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
33	PRG_ALRM1	Programmable Alarm 1 *MSA Default: HIPWR_ON*	O	3.3V LVCMOS	Active High per MDIO document [5]		
34	PRG_ALRM2	Programmable Alarm 2 *MSA Default: MOD_READY, Ready state has been reached*	O	3.3V LVCMOS	Active High per MDIO document [5]		
35	PRG_ALRM3	Programmable Alarm 3 *MSA Default: MOD_FAULT*	O	3.3V LVCMOS	Active High per MDIO document [5]		
38	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull – Down[4]
40	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	

2.4 Hardware Alarm Pins: Functional Description

2.4.1 Programmable Alarms (PRG_ALRMs)

These alarm pins allow for the system to program module supported alarms to Hardware pins. The intention is to allow for maximum design and debug flexibility.

2.4.1.1 Programmable Alarm 1 Pin

Programmable Alarm Pin 1 (PRG_ALRM1) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be High Power On (HIPWR_ON) indicator with active-high logic.

The 40G and 100G applications for which the CFP is designed have numerous PMDs or port types which require specialized optoelectronic components which dissipate significant electrical power. The CFP MSA is designating that there be an intermediate state between the Low-Power state to the Module-Ready state, the TX-Off state. This state and default alarm function provides a defined state and signal where the CFP

[4] Pull-Down resistor (<100Ohm) is located within the CFP module. Pull-up should be located on the host.

module is asserting wavelength control mechanisms and other high power functions. This default function signals the host system that the CFP module is now ready for the transmitter to be enabled. See section 2.8 for background information on start-up sequence or refer to the “CFP MSA Management Interface Specification” for details.

2.4.1.2 Programmable Alarm 2 Pin

Programmable Alarm Pin 2 (PRG_ALRM2) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be Module Ready (MOD_READY) indicator with active-high logic.

The default function MOD_READY is used by the CFP MSA during the module initialization. When asserted it indicates that the module has completed the necessary initialization process and is ready to transmit and receive data. See section 2.8 for background information on start-up sequence or refer to the “CFP MSA Management Interface Specification” for details.

2.4.1.3 Programmable Alarm 3 Pin

Programmable Alarm Pin 3 (PRG_ALRM3) is an output pin to the Host, operating with programmable logic. It can be re-programmed over MDIO registers to another MDIO alarm register while the module is in any steady state except Reset. MSA specifies the default function to be Module Fault (MOD_FAULT) indicator with active-high logic.

The default function MOD_FAULT is used by the CFP MSA during the module initialization. When asserted it indicates that the module has entered into a Fault state. See section 2.8 for background information on start-up sequence or refer to the “CFP MSA Management Interface Specification” for details.

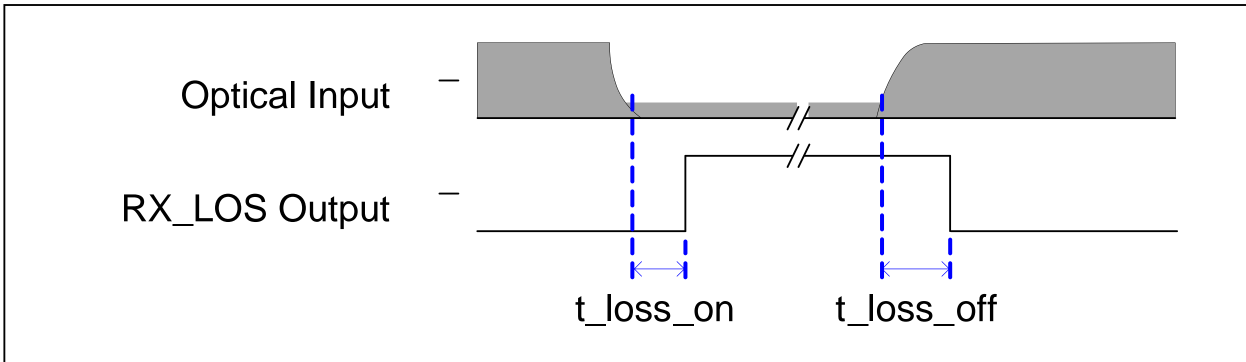
2.4.2 Module Absent Pin

Module Absent Pin (MOD_ABS) is an output pin from CFP to Host. It is pulled up on the host board and is pulled down to ground in the CFP module. MOD_ABS asserts a “Low” condition when module is plugged in host slot. MOD_ABS is asserted “High” when the CFP module is physically absent from a host slot.

2.4.3 Receiver Loss of Signal Pin

The Receiver Loss of Signal Pin (RX_LOS) is an output pin to the Host, operating with active-high logic. When asserted, it indicates received optical power in the CFP module is lower than the expected value. The optical power at which RX_LOS is asserted may be specified by other governing documents and the CFP module vendor as the alarm threshold level is application specific. The RX_LOS is the logic OR of the LOS signals from all the input receiving channels in a CFP module.

Figure 2-3: Receiver Loss of Signal Timing Diagram



2.5 Management Interface Pins (MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP MDIO electrical interface consists of 8 pins including 2 pins for MDC and MDIO, 5 Physical Port Address pins, and the Global Alarm pin. MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP MDIO pins are listed in Table 2-4: Management Interface Pins.

Table 2-4: Management Interface Pins (MDIO)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
41	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
47	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
48	MDC	MDIO Clock	I	1.2V LVCMOS			
46	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per MDIO document [5]		
45	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
44	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			
43	PRTADR3	MDIO Physical Port address bit 3	I	1.2V LVCMOS			
42	PRTADR4	MDIO Physical Port address bit 4	I	1.2V LVCMOS			

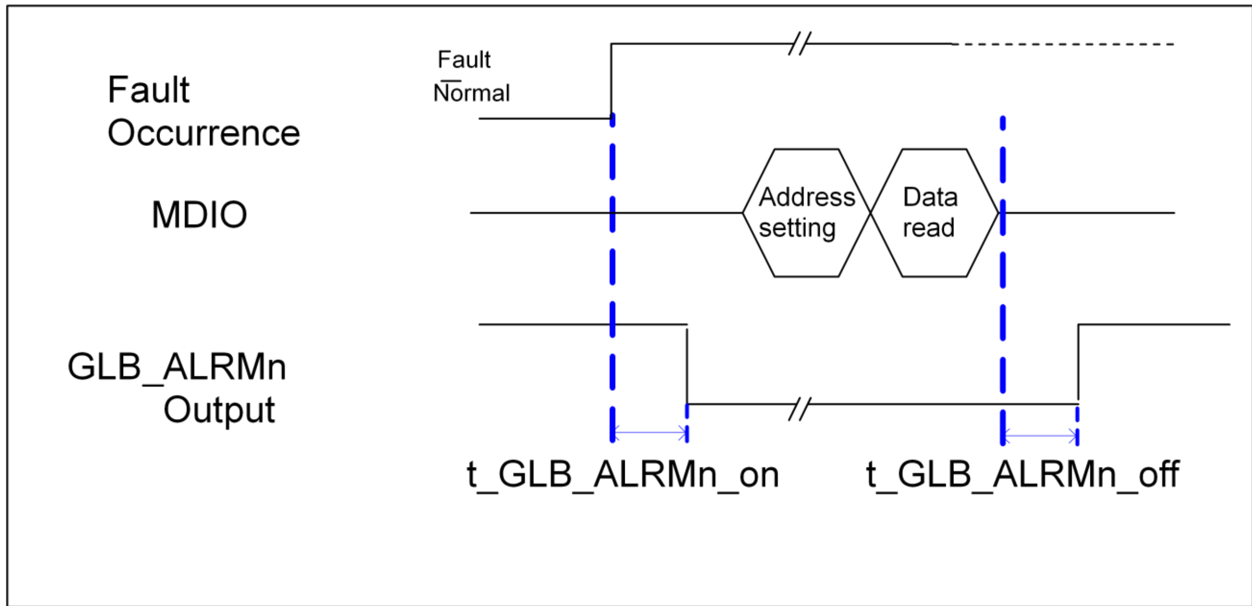
2.6 CFP Management Interface Hardware Description

2.6.1 Global Alarm Pin

Global Alarm Pin (GLB_ALRMn) is an output pin to the Host, operating with active-low logic. When GLB_ALRMn is asserted (driven low), it indicates that a Fault/Alarm/Warning/Status (FAWS) condition has occurred. It is driven by the logical OR of all fault/status/alarm/warning conditions latched in the latched registers. Masking Registers are provided so that GLB_ALRMn may be programmed to assert only for specific fault/alarm/warning/status conditions. It is recommended that the Host board be designed to support a high priority event handling service to respond to the assertion of this pin. Upon the assertion

(driven low) of this pin, the Host event handler identifies the source of the fault by reading the latched registers over the MDIO interface. The reading action clears the latched registers which in turn causes the CFP to de-assert (releases) the GLB_ALRMn pin.

Figure 2-4: Global Alarm Timing Diagram[5]



For more detail on the GLB_ALRMn pin please refer to the "CFP MSA Management Interface Specification".

2.6.2 MDIO Pin

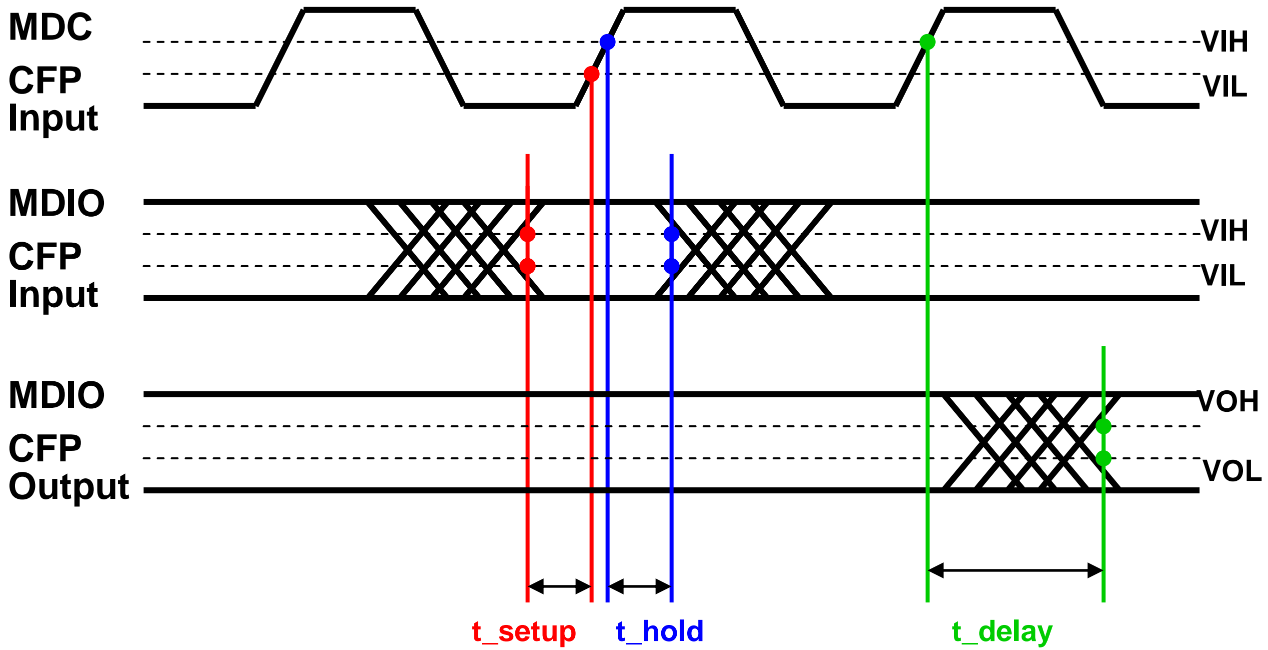
The MDIO specification is defined in clause 45 of the IEEE 802.3 Standard. The CFP Module shall support 4.0 Mbit/s as maximum data rate. The CFP uses an MDIO with 1.2V LVCMOS logic levels.

2.6.3 MDC Pin

Host specifies a maximum MDC rate of 4.0 MHz and CFP module hence has to support a maximum MDC rate up to 4.0 MHz. The CFP MSA module shall support a minimal 10 ns setup and hold time in its MDIO implementation.

[5] In this figure the Fault Occurrence is shown transitioning to a "Normal" Status. In order for this transition to occur a read of the alarmed register must have occurred such that the fault has been serviced.

Figure 2-5: MDIO & MDC Timing Diagram



2.6.4 MDIO Physical Port Addresses

These control pins are used for the system to address all of the CFP ports contained within a host system. PRTADR0 corresponds to the LSB in the physical port addressing scheme. The 5-wire Physical Port Address lines are driven by host to set the module Physical Port Address which should match the address specified in the MDIO Frame. It is recommended that the Physical Port Addresses not be changed while the CFP module is powered on.

2.7 Hardware Signal Pin Electrical Specifications

2.7.1 Control & Alarm Pins: 3.3V LVCMOS Electrical Characteristics

The hardware control and alarm pins specified as 3.3V LVCMOS functionally described above shall meet the characteristics described in table 2-5. Reference figures are provided regarding pin termination; see figure 2-7 and figure 2-8.

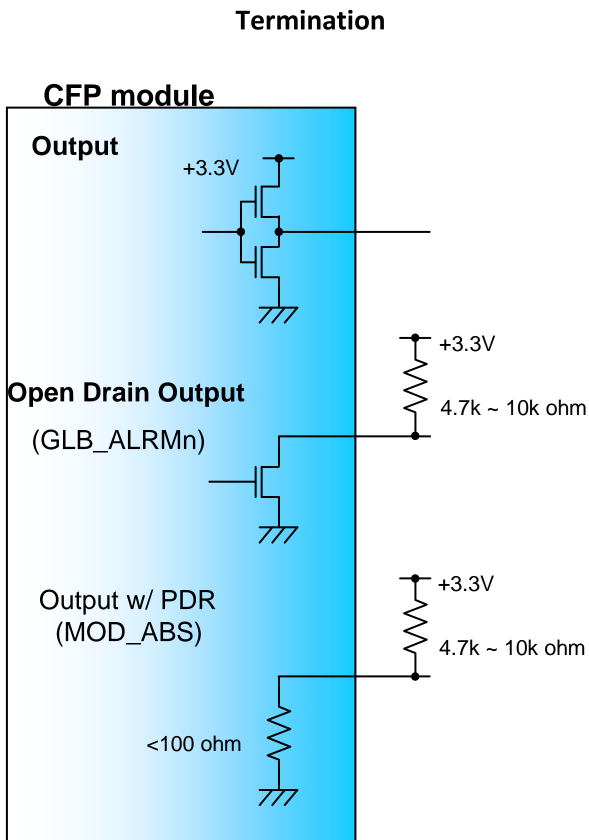
Table 2-5: 3.3V LVCMOS Electrical Characteristics[6]

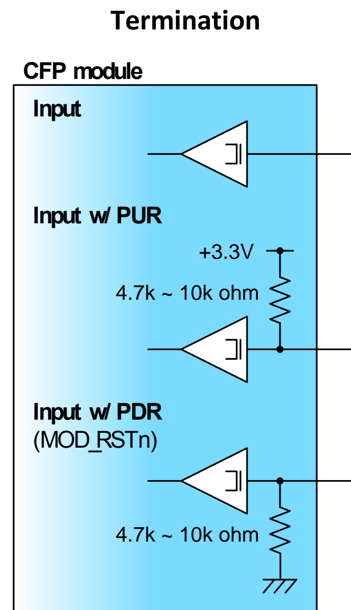
Parameters	Symbol	Min	Typ.	Max	Unit
Supply Voltage	VCC	3.2	3.3	3.4	V
Input High Voltage	VIH	2	-	VCC + 0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V
Input Leakage Current	IIN	-10	-	+10	uA
Output High Voltage (I_{OH}=-100uA)	VOH	VCC – 0.2	-	-	V
Output Low Voltage (I_{OL}=100uA)	VOL	-	-	0.2	V
Minimum Pulse Width of Control Pin Signal	t_CNTL	100			us

[6] Based on XFP MSA specification and JEDEC No.8C.01

Figure 2-6: Reference +3.3V LVCMOS Output Termination

Figure 2-7: Reference +3.3V LVCMOS Input Termination





2.7.2 *MDIO Interface Pins: 1.2V LVCMOS Electrical Characteristics*

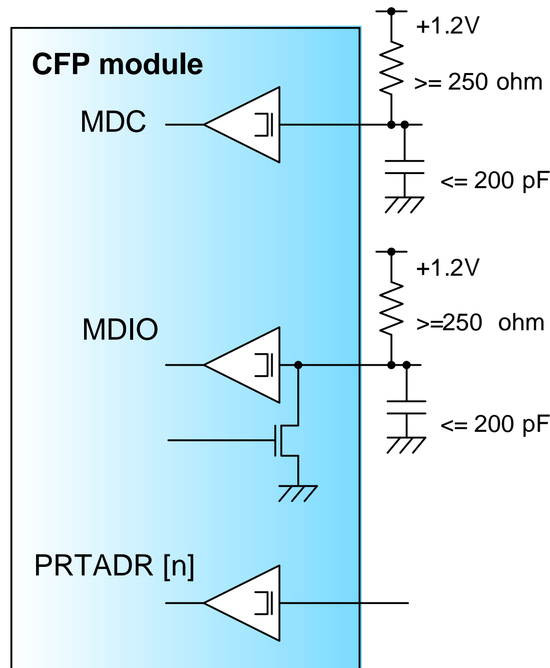
The MDIO interface pins specified as 1.2V LVCMOS functionally described above shall meet the characteristics described in Table 2-6. Reference figures are provided regarding pin termination; see Figure 2-8.

Table 2-6: 1.2V LVCMOS Electrical Characteristics[7]

Parameters	Symbol	Min	Typ.	Max	Unit
Input High Voltage	VIH	0.84	-	1.5	V
Input Low Voltage	VIL	-0.3	-	0.36	V
Input Leakage Current	IIN	-100	-	+100	uA
Output High Voltage	VOH	1.0	-	1.5	V
Output Low Voltage	VOL	-0.3	-	0.2	V
Output High Current	IOH	-	-	-4	mA
Output Low Current	IOL	+4	-	-	mA
Input capacitance	Ci	-	-	10	pF

[7] Based on IEEE 802.3ae 45.5.5.16 Electrical Characteristics

Figure 2-8: Reference MDIO Interface Termination[8]



2.8 Hardware Signaling Pin Timing Requirements

The CFP MSA module is designed to have a tightly coupled interface with host systems. Accordingly, the CFP MSA has defined a start-up sequence with steady state conditions, transient state conditions, and associated signaling flags to indicate state transition. A reference diagram of the start-up is shown in Figure 2-9 below. For a full description of the CFP MSA Start-Up sequence please refer to the "CFP MSA Management Interface Specification".

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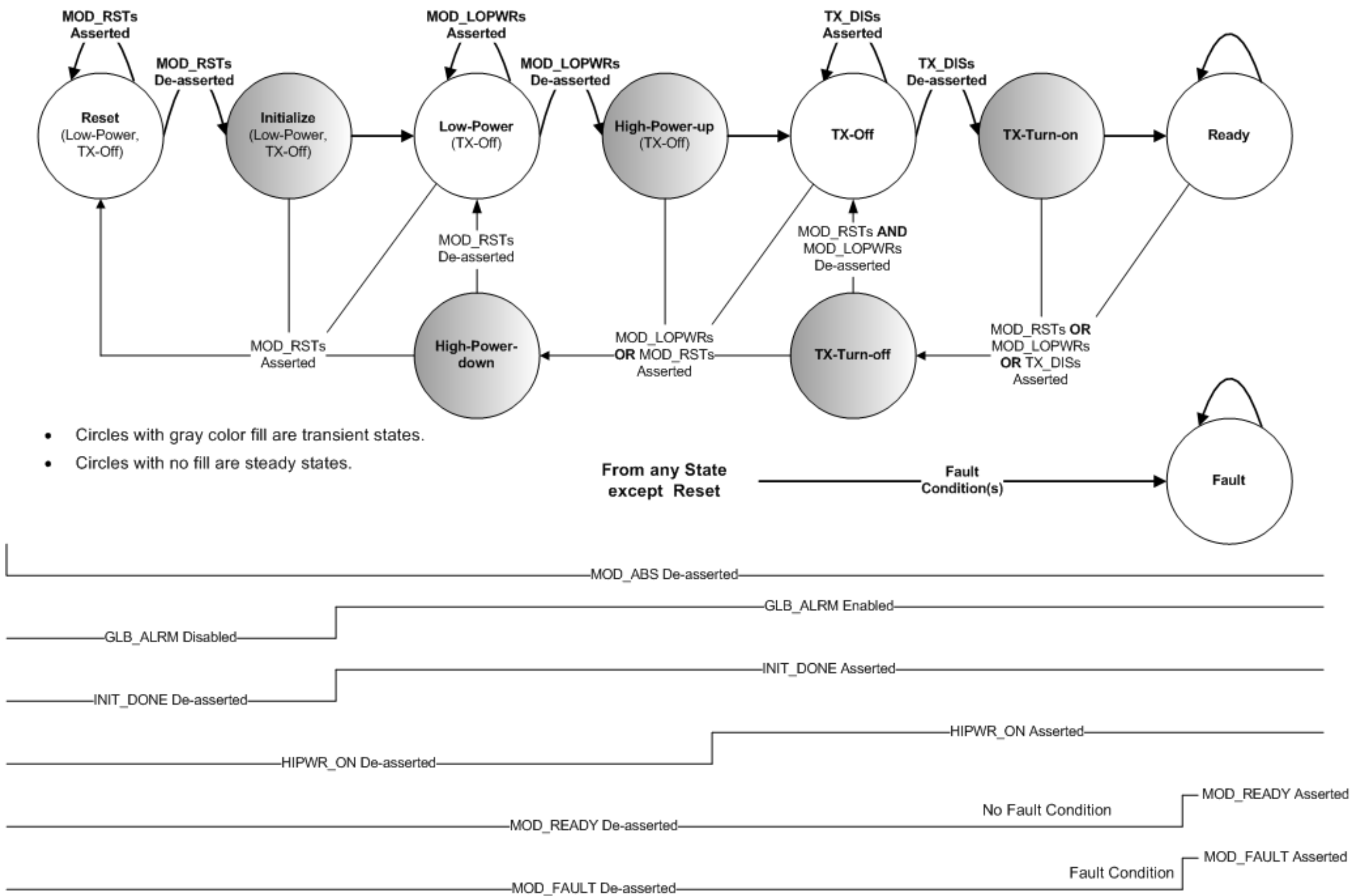
[8] The MSA recommends host termination resistor value of 560 Ohms, which provides the best balance of performance for both open-drain and active tri-state driver in the module. Host termination resistor values below 560Ohms are allowed, to a minimum of 250 Ohms, but this degrades active driver performance. Host termination resistor values above 560 Ohms are allowed but this degrades open-drain driver performance.

The above drawings, with maximum host load capacitance of 200pF, also define the measurement set-up for module MDC timing verification

Figure 2-9: CFP MSA Start-Up Flow Diagram



The CFP MSA module is designed to support a diverse set of high speed applications. The CFP MSA defines some timing parameters explicitly which are dependent upon the form factor. However, many of the timing parameters often used in optical networking applications are application specific. Accordingly, it is recommended that these timing parameters are specified by the CFP MSA module vendor.

2.8.1 INIT_DONE

The INIT_DONE signal is a required internal gating signal which may be used for multiple functions internal to the CFP MSA module. This internal signal is responsible for: (a) holding GLB_ALRM de-asserted (open); (b) holding MDIO inactive; (c) holding Hardware Alarms de-asserted; until the module has completed the Initialize state.

Table 2-7: Timing Parameters for CFP Hardware Signal Pins

Parameter	Symbol	Min.	Max.	Unit	Notes & Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	Application Specific. May depend on current state condition when signal is applied. See Vendor Data Sheet
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_deassert			ms	Value is dependent upon module start-up time. Please see register "Maximum High-Power-up Time" in "CFP MSA Management Interface Specification"
Receiver Loss of Signal Assert Time	t_loss_assert		100	µs	Maximum value designed to support telecom applications
Receiver Loss of Signal De-Assert Time	t_loss_deassert		100	µs	Maximum value designed to support telecom applications
Global Alarm Assert Delay Time	GLB_ALRMn_assert		150	ms	This is a logical "OR" of associated MDIO alarm & status registers. Please see MDIO document for further details
Global Alarm De-Assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of associated MDIO alarm & status registers. Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled (TX_DIS asserted)	t_deassert		100	µs	Application Specific
Transmitter Enabled (TX_DIS de-asserted)	t_assert		100	ms	Value is dependent upon module start-up time. Please see register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

3 MODULE MANAGEMENT INTERFACE DESCRIPTION

The CFP module utilizes MDIO IEEE 802.3 clause 45 for its management interface. The CFP MDIO implementation is defined in a separate document entitled, "CFP MSA Management Interface Specification". When multiple CFP modules are connected via a single bus, a particular CFP module can be selected by using the Physical Port Address pins.

4 PERFORMANCE SPECIFICATIONS

4.1 OPERATING ENVIRONMENT

For the CFP module all minimum and maximum parameters are specified End-of-Life within the overall relevant operating case temperature range from 0°C to 70°C unless otherwise stated.
The typical values are referenced to +25°C, nominal power supply, Beginning-of-Life.

Host systems must use the appropriate cooling system to keep the case temperature within the recommended operating limits.

CFP module vendors must supply a maximum case temperature reference point as this value will vary across PMD and port type as well as across CFP vendors.

The CFP modules and the host system are hot-pluggable. The module or the host system shall not be damaged by insertion or removal of the module.

4.2 POWER SUPPLIES AND POWER DISSIPATION

4.2.1 Voltage power supply and power dissipation

The CFP module requires a single power supply. Longer optical reach modules require larger currents than shorter optical reach modules. It is recommended that system designers thermally budget for the maximum power dissipation as longer optical reach modules will dissipate more power than shorter optical reach modules. Please refer to Appendix I: THERMAL DESIGN for more details on the thermal characteristics.

4.2.2 Inrush current

The inrush current on the 3.3V power supply shall be limited by the CFP module to assure a maximum rate of change defined in table 4-1 below.

4.2.3 Turn-off current

The CFP MSA module supports a variety of applications many of which require high power dissipation and large current draws on the 3.3V power supply. As noted in section 2.2.3, the MOD_LOPWR pin is 1mm shorter than Vcc pins to provide the module a signal to allow for smooth ramp down of the power supply current. The module shall limit the turn-off current to assure a maximum rate of change per table 4-1 below. In addition the host may use MOD_ABS pin, which is also 1mm shorter than Vcc to respond to the module transitioning to low power state.

4.2.4 Power Supply Noise Susceptibility

A host system will supply stable power to the module and guarantee that noise & ripple on the power supply does not exceed that defined in the table. A possible example of a power supply filtering circuit that might be used on the host system is a PI (proportional integral) C-L-C filter. A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3V power supply which is less than that defined in the table 4-1. The component values of power supply noise filtering circuit, such as the

capacitor and inductor, must be selected such that maximum Inrush and Turn-off current does not cause voltage transients which exceed the absolute maximum power supply voltage, all specified in Table 4-1.

Table 4-1 Voltage power supply

Parameters		Symbol	Min	Typ.	Max	Unit
Absolute Maximum Power Supply Voltage		VCC			3.6	V
Operating Power Supply	Voltage	VCC	3.2	3.3	3.4	V
	Current[9]	ICC	-	-	10	A
Total Power Dissipation	Class 1	Pw	-	-	8	W
	Class 2				16	
	Class 3				24	
	Class 4				32	
Low Power Mode Dissipation		Plow			2	W
Inrush Current	Class 1 and Class 2	I-inrush			50	mA/usec
Turn-off Current		I-turnoff	-50			mA/usec
Inrush Current	Class 3 and Class 4	I-inrush			100	mA/usec
Turn-off Current		I-turnoff	-100			mA/usec
Power Supply Noise		Vrip			2% 3%	DC – 1MHz 1 – 10MHz

4.2.5 Grounding

There are two types of ground signals listed in the CFP 148 pin connector description: 3.3V_GND; and GND. These two grounds may be tied together. The guide rails, connector cover and assorted mechanicals are all frame or chassis GND. Do not connect this ground to the module signal ground.

4.3 OPTICAL CHARACTERISTICS

4.3.1 Optical specifications

The CFP module will comply with standardized optical specifications such as the optical reaches specified in IEEE for datacom applications,or in ITU-T for Telecom applications. Some of the relevant reference documents are: IEEE 802.3ba, Telcordia GR-253, ITU-T G.691, ITU-T G.692, ITU-T G.693, and ITU-T G.959, ITU-T G.709.

4.3.1.1 Ethernet Optical specifications

For Ethernet applications the module shall comply with the optical parameter tables specified in IEEE 802.3 clauses 86, 87 and 88.

4.3.1.2 Telecom Optical specifications

For Telecom applications the module is recommended to comply with the optical parameter tables specified in G.693, G.959.1

[9] Maximum current per pin shall not exceed 500mA.

4.3.1.2.1 Optical WDM Grid

CFP MSA modules may operate within specific WDM (wavelength division multiplexed) grids. It is recommended that CFP MSA modules adhere to the ITU-T WDM grid conventions.
The ITU-T document G.694.1 specifies the DWDM frequency grid anchored to 193.1 THz. It supports a variety of channel spacing of 12.5, 25, 50, 100 GHz and wider.

The ITU-T document G.694.2 specifies the CWDM wavelength grid, which supports a channel spacing of 20 nm. Unlike DWDM, whose grid is specified in terms of an anchor frequency, the CWDM grid is defined in terms of wavelength separation. This grid is made up of 18 wavelengths defined within the range 1271 nm to 1611 nm.

4.3.2 Testing Method

For Ethernet applications, it is suggested that the CFP module be tested per the optical test methods outlined in IEEE 802.3 clauses 86, 87 and 88.

4.4 HIGH SPEED ELECTRICAL CHARACTERISTICS

The high speed electrical interface shall be AC coupled within the module as is shown in Figure 4-1: High Speed I/O for Data and Clocks.

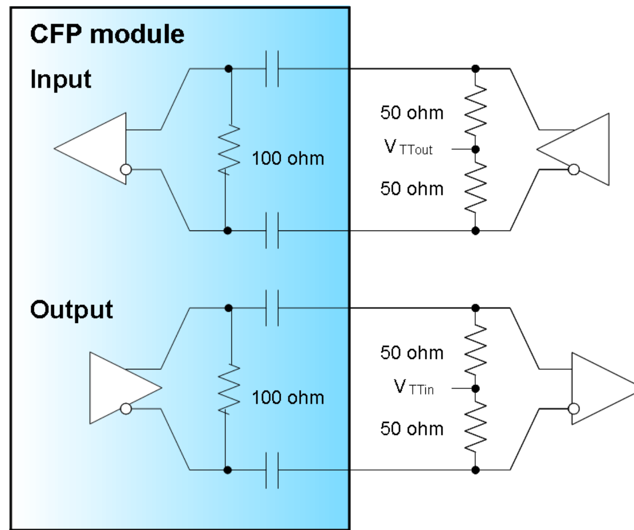
4.4.1 Transmitter Data (and Clock)

The Transmitter Data is defined in IEEE P802.3ba Annex 83A and Annex 83B defining CAUI and XLAUI. The Figure 4-1: High Speed I/O shows the recommended termination for these circuits. Alternate signaling logic are OTL3.4 and OTL4.10 which are specified in [11] ITU-T RECOMMENDATION G.709, Amendment 3. Lane orientation and designation is specified in the pin-map tables Table 5-6 and Table 6-1.

4.4.2 Receiver Data (and Clock)

The Receiver Data is defined in IEEE P802.3ba Annex 83A and Annex 83B defining CAUI and XLAUI. The Figure 4-1: High Speed I/O shows the recommended termination for these circuits. Alternate signaling logic are OTL3.4 and OTL4.10 which are specified in [11] ITU-T RECOMMENDATION G.709, Amendment 3. Lane orientation and designation is specified in the pin-map tables Table 5-6, and Table 6-1.

1 Figure 4-1: High Speed I/O for Data and Clocks



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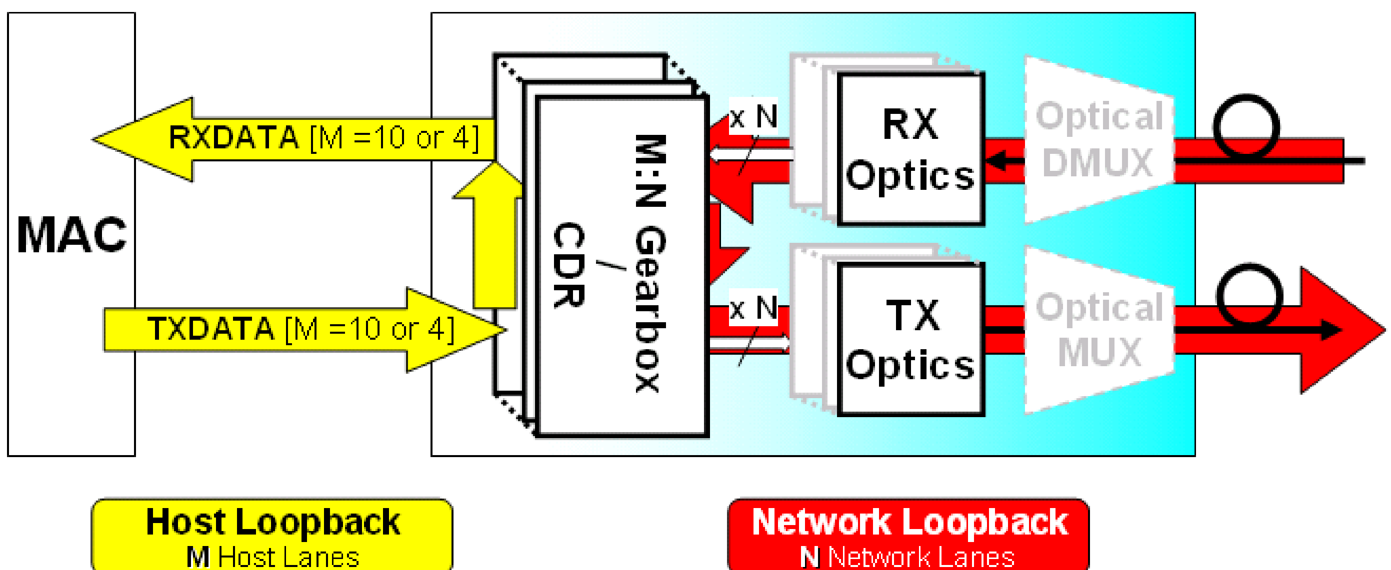
4 ### *4.4.3 Loopback (Optional)*

5 The CFP module may support loopback functionality. Loopback commands are accessed via the MDIO
6 management interface. Suggested loopback orientation implementation is TX0 to RX0. The host loopback
7 and the network loopback are oriented per Figure 4-2 shown below. Host loopback loops the 'M' host lanes.
8 Network loopback loops the 'N' network lanes. The capability to support the loopback functionality is
9 dependent upon the interface IC technology labeled as "Gearbox/CDR" in the figure. The capability of this
10 block is application dependent. If PRBS checkers and generators are supported, they will be located in the
11 "Gearbox/CDR" block. The CFP MSA module vendor will specify which loopback functionality, if any, is
12 available. For details on controlling the loopback mode, please refer to "CFP MSA Management Interface
13 Specification".
14

15 Figure 4-2: Optional Loopback Orientation



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17

4.4.4 Reference Clock

The host shall supply a reference clock (REFCLK) at 1/64 electrical lane rate. The CFP module may optionally use the 1/64 reference clock for transmitter path retiming, for example for Ethernet applications.

The host shall optionally supply a reference clock (REFCLK) at 1/16 electrical lane rate,. The CFP module may optionally use the 1/16 reference clock for transmitter path retiming, for example for Telecom applications.

The REFCLK shall be CML differential AC coupled and terminated within the CFP module as shown in Figure 4-1: High Speed I/O for Data and Clocks. There is no required phase relationship between the data lanes and the reference clock, but the clock frequency shall not deviate more than specified in Table 4-2. For detailed clock characteristics please refer to the below table.

REFCLK is not intended for use in the receiver path. If required, the CFP module has to provide a clock reference generated internally.

Table 4-2: Reference Clock Characteristics

		Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4: CFP Module Clocking Signals
Frequency Stability	Δf	-100		100	ppm	For Ethernet applications;
		-20		20		For Telecom applications
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
RMS Jitter[10],[11]	σ			10	ps	Random Jitter. Over frequency band of 10kHz < f < 10MHz
Clock Duty Cycle		40		60	%	
Clock Rise/Fall Time 10/90%	$t_{r/f}$	200		1250	ps	1/64 of electrical lane rate
		50		315		1/16 of electrical lane rate

4.4.5 Transmitter Monitor Clock (Option)

The CFP module may supply an optional transmitter monitor clock. This clock is intended to be used as a reference for measurements of the optical output. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data. Clock termination is shown in Figure 4-1. Detailed clock characteristics are specified in Table 4-3.

4.4.6 Receiver Monitor Clock (Option)

The CFP module may supply an optional receiver monitor clock. This clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a rate relative to the

[10] The spectrum of the jitter within this frequency band is undefined. The CFP shall meet performance requirements with worst case condition of a single jitter tone of 10ps RMS at any frequency between 10KHz and 10MHz

[11] For Telecom applications better frequency may be required.

optical lane rate of 1/16 rate for 40Gbit/s applications and 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 rate of the receiver electrical output data. Clock termination is shown in Figure 4-1. Detailed clock characteristics are specified in Table 4-3.

Table 4-3: Optional Transmitter & Receiver Monitor Clock Characteristics

		Min.	Typ.	Max.	Unit	Notes
Impedance	Zd	80	100	120	Ω	
Frequency						See Table 4-4: CFP Module Clocking Signals
Output Differential Voltage	V_{DIFF}	400		1200	mV	Peak to Peak Differential
Clock Duty Cycle		40		60	%	

Table 4-4: CFP Module Clocking Signals

Clock Name	Status	I/O	Default rate			Optional rate
			M ≠ N Datacom 100GBASE-LR4 100GBASE-ER4 40GBASE-FR[12,13]	**M = N** 100GBASE-SR10 40GBASE-SR4 40GBASE-LR4	**M ≠ N Telecom** OC-768, OTN (40G,43G)	
REFCLK	Required	I	1/64 of host lane rate	1/64 of host lane rate	1/64 of host lane rate	1/16 of host lane rate
TX_MCLK	*Optional*	*O*	1/8 of network lane rate	1/16 of network lane rate	1/16 of network lane rate	1/16, 1/64 of host lane rate
RX_MCLK	*Optional*	*O*	1/8 of network lane rate	1/16 of network lane rate	1/16 of network lane rate	1/16, 1/64 of host lane rate

[12] The term “40GBASE-FR” is the 40GbE serial optical interface in the task force phase at IEEE-SA at the time of this publication. Also, 1/16 of optical lane rate clock is recommended for TX_MCLK and RX_MCLK.

[13] Multi-protocol modules are recommended to adopt the clock rate used in Telecom applications.

Figure 4-3: Example of clocking for M=N applications

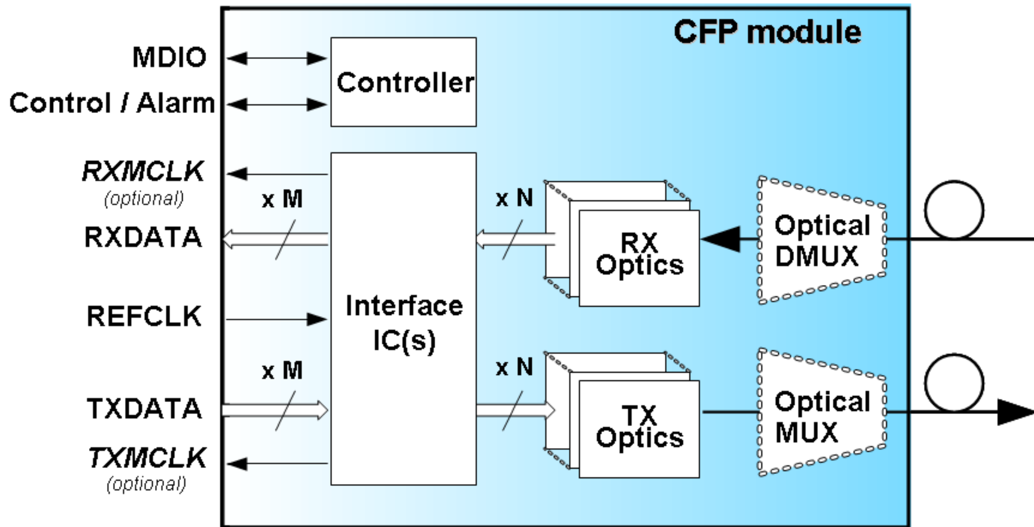
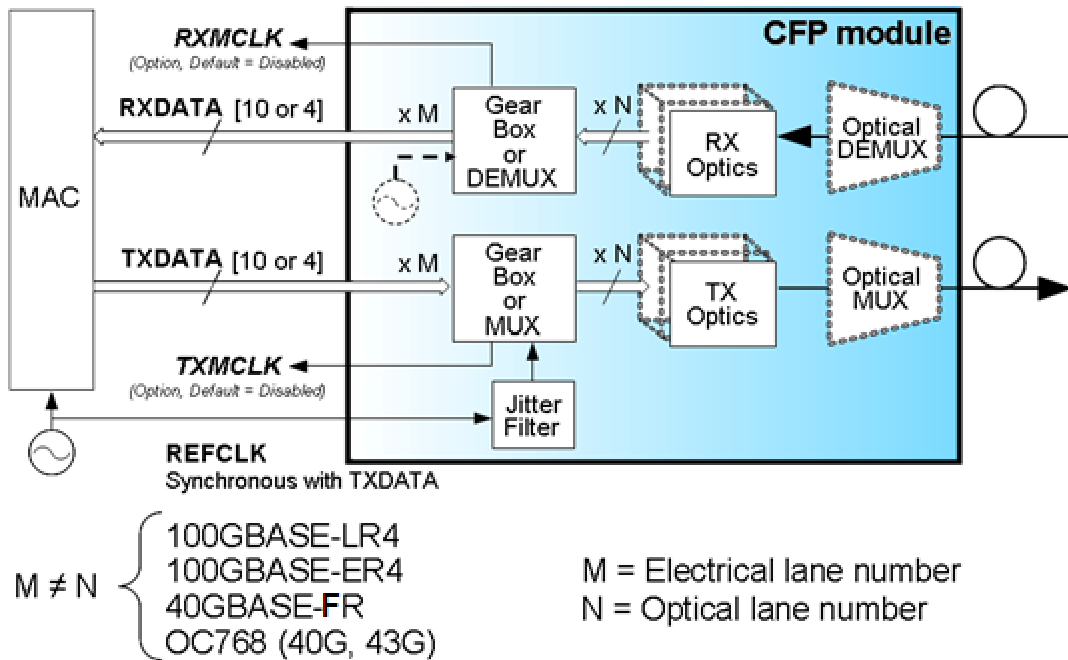
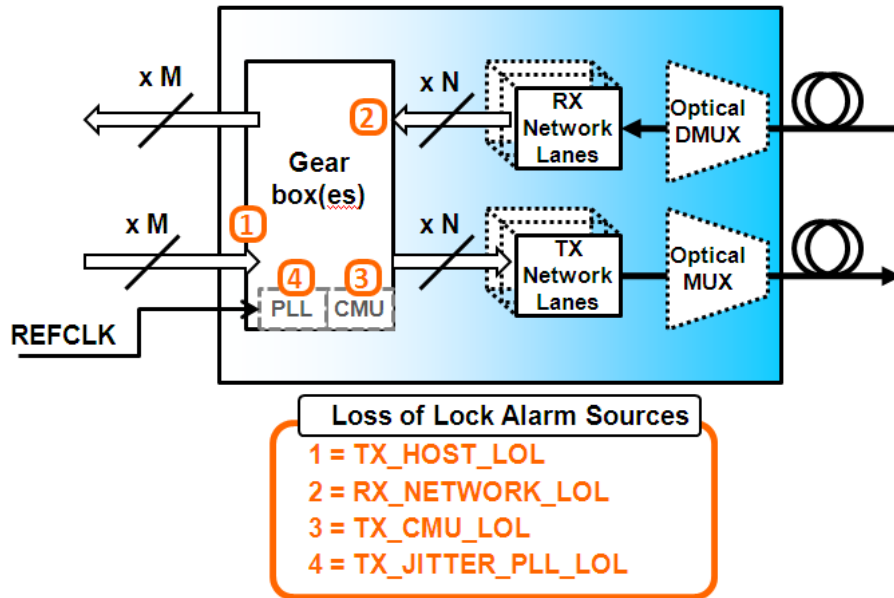


Figure 4-4: Example of clocking for M≠N applications[14]



[14] Use of oscillator for receiver reference clock is application dependent

Figure 4-5: Loss of Lock Alarm Sources

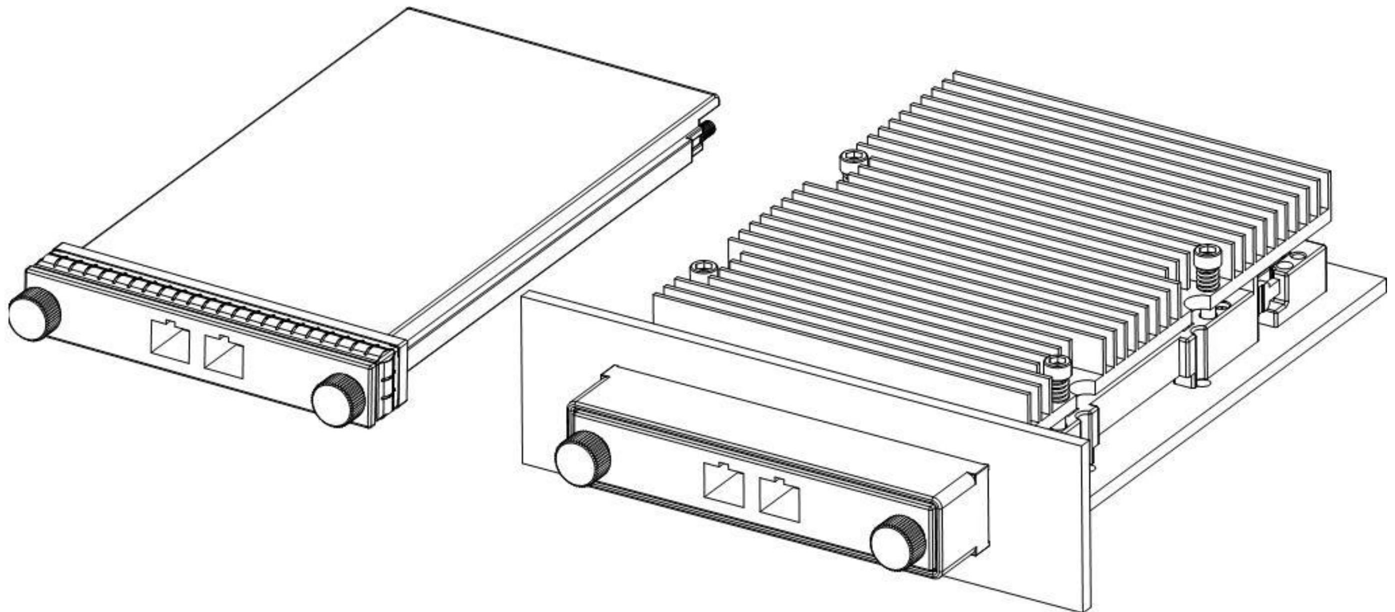


5 MECHANICAL SPECIFICATIONS

5.1 Mechanical Overview

The CFP MSA module is designed to be assembled into a host system with a railing system. The railing system assembly is fabricated within the host system, and the CFP MSA module may be inserted at a later time. Shown in Figure 5-1 is a drawing of the CFP module and a CFP module inserted into a host system with a riding heat sink.

Figure 5-1: CFP Module & CFP Module Mated in Host System



Starting in Figure 5-2, is an overview of the mechanical assembly with the subsequent figures show the constituent elements in greater detail. The final dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

Figure 5-2: Railing System Overview

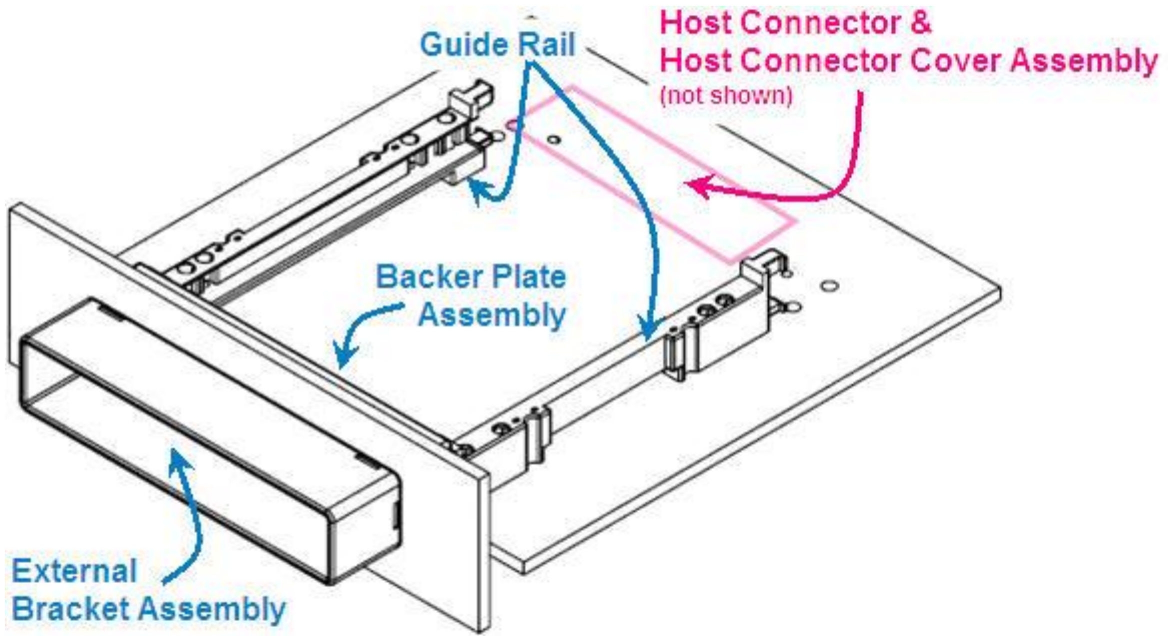


Figure 5-3: External Bracket Assembly

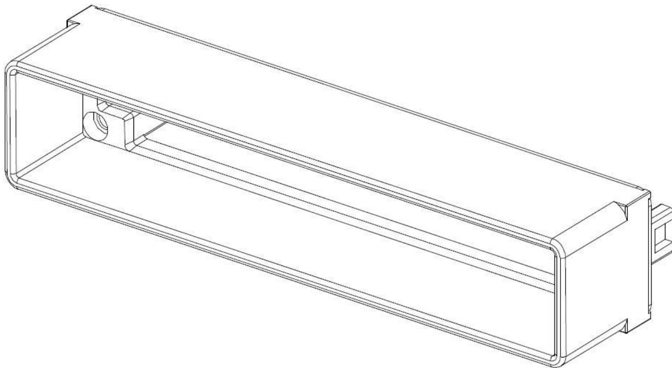


Figure 5-4: Backer Plate Assembly

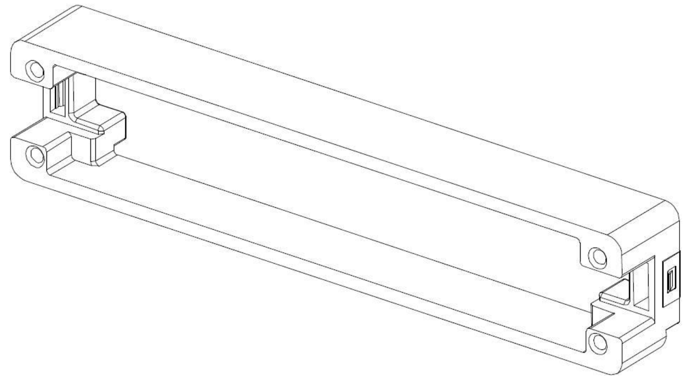
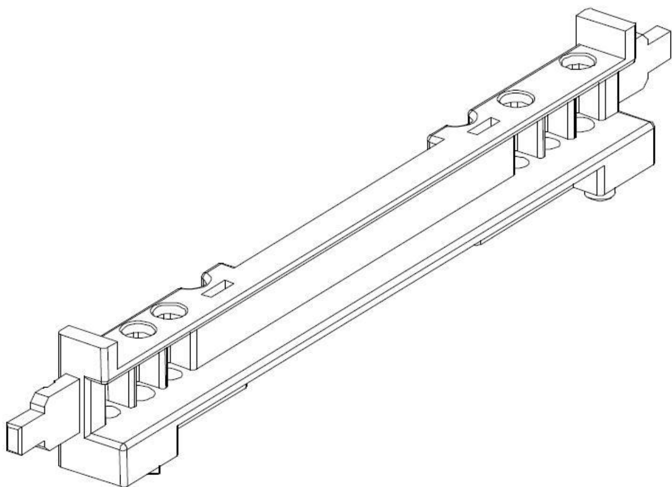


Figure 5-5: Guide Rail



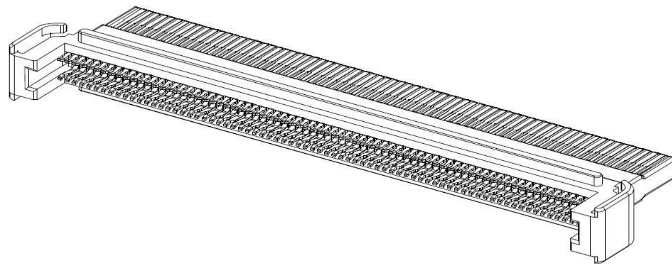
5.2 Electrical Connector

Shown below is detail on the electrical connector system used for the CFP MSA. The final dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

5.2.1 Module Plug Connector

The CFP MSA is specifying a two piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-6 is the module plug connector assembly which is contained as a sub-component within the CFP module.

Figure 5-6: Module Plug Connector Assembly



5.2.2 Host Connector

The CFP MSA is specifying a two piece electrical connector for superior electrical performance and superior mechanical integrity. Shown in Figure 5-7 and Figure 5-8 are overview drawings of the host connector assembly. This assembly shall be built into the host system. The Host Connector shall be covered by the Host Connector Cover Assembly and provides an electromagnetic shielding as well as a solid mechanical interface for the module fastening screws.

Figure 5-7: Host Connector Cover Assembly

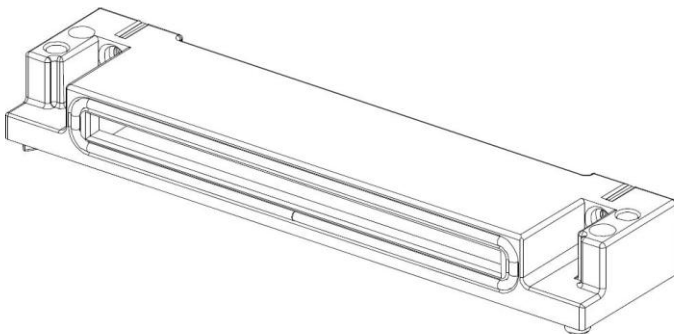
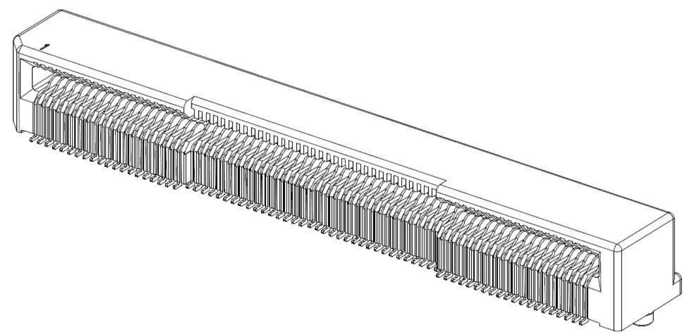


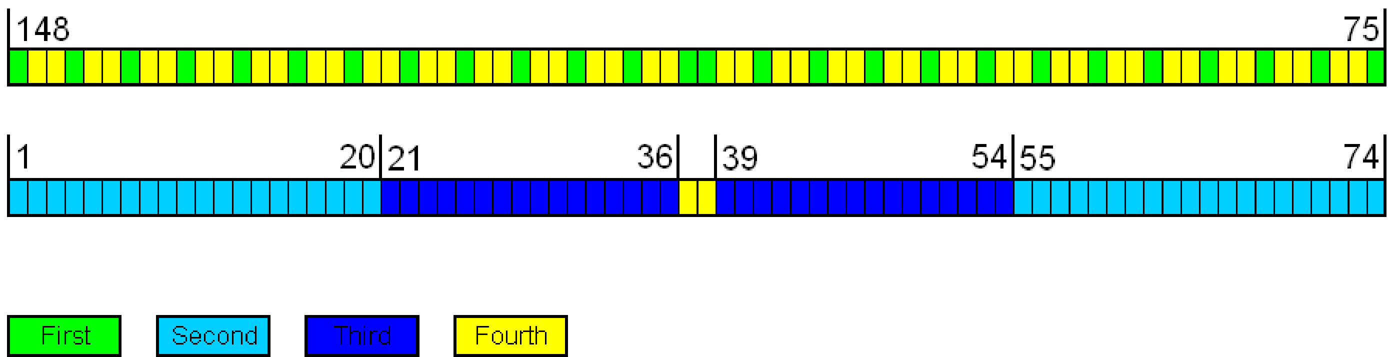
Figure 5-8: Host Connector



5.2.3 *Connector Pin Contact Mating*

The host connector has a physical offset of metal contact pins to insure that certain signals make engagement between the module and host prior to other signals. There are four categories of pin engagement. A map of the connector engagement is shown in Figure 5-9. The connector pin map engagement order is guaranteed by the physical offset built into the host connector. The module plug connector has all contacts on the same plane without offset.

Figure 5-9: Pin Map Connector Engagement



5.3 Module Dimensions

The detailed CFP module dimensions are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

Table 5-1: CFP Mechanical Characteristics

	Max.	Unit	Notes
Weight	350	g	
Flatness	0.15	mm	
Roughness	6.3	Ra	

5.3.1 *CFP Mechanical Surface Characteristics*

The mechanical surface of flat top CFP module which may be in contact with the host riding heat sink assembly shall be compliant with specifications in Table 5-1. Non compliance to these specifications may cause significant thermal performance degradation.

5.3.2 *CFP Insertion & Extraction*

As described in 1.3.1, CFP module shall be hot pluggable. A consequence of the CFP module being hot pluggable is that an end user be equipped to insert and extract the module in the field. The required forces are specified below in Table 5-2.

Table 5-2: Insertion, Extraction Forces

	Max.	Unit	Notes
Maximum Insertion Force	80	N	
Maximum Extraction Force	80	N	
Minimum Retention Force	130	N	With Captive Screw engaged
Fastener Torque	1.0	Nm	3mm captive screw

5.4 Host System Dimensions

The detailed CFP host system dimensions including host board layout are located in a separate document hosted on the CFP MSA Website (www.cfp-msa.org).

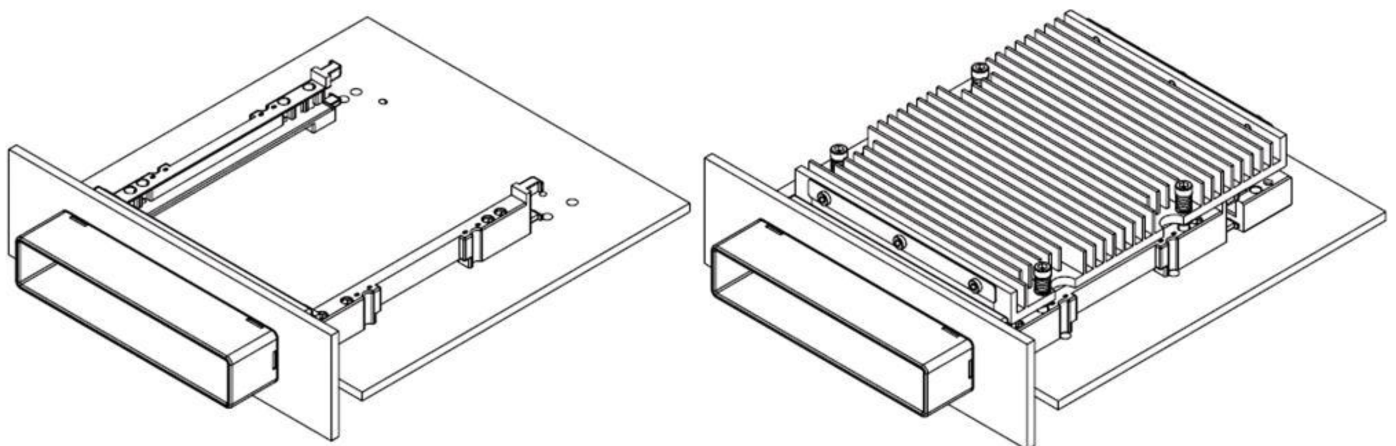
5.5 Riding Heat Sink

Since the CFP MSA module is being designed to support a wide array of optical networking applications, it may be necessary to provide a heat sink system which allows for system customization. The CFP MSA is providing a Riding Heat Sink system definition to allow system designers the maximum flexibility for their system while maintaining a common form factor and faceplate aperture across systems.

As shown in Figure 5-10, the heat sink is mounted to the host railing system. It is recommended that the heat sink be mounted with a spring load to provide positive force, but that the overall travel in the y-axis be minimized. For a more detailed discussion, please refer to Appendix I: THERMAL DESIGN .

The heat sink illustrated in Figure 5-10 is for reference only. The recommended material for the heat sink is aluminum. Furthermore, a thermal interposer for reduced friction is recommended to be used on the underside of the riding heat sink.

Figure 5-10: Riding Heat Sink Overview



The mounting dimensions for the Riding Heat Sink are shown below in Figure 5-11. The actual dimensions of the heat sink shall be optimized for the particular host system. For a more detailed discussion, please refer to Appendix I: THERMAL DESIGN .

Figure 5-11: Riding Heat Sink Dimensions

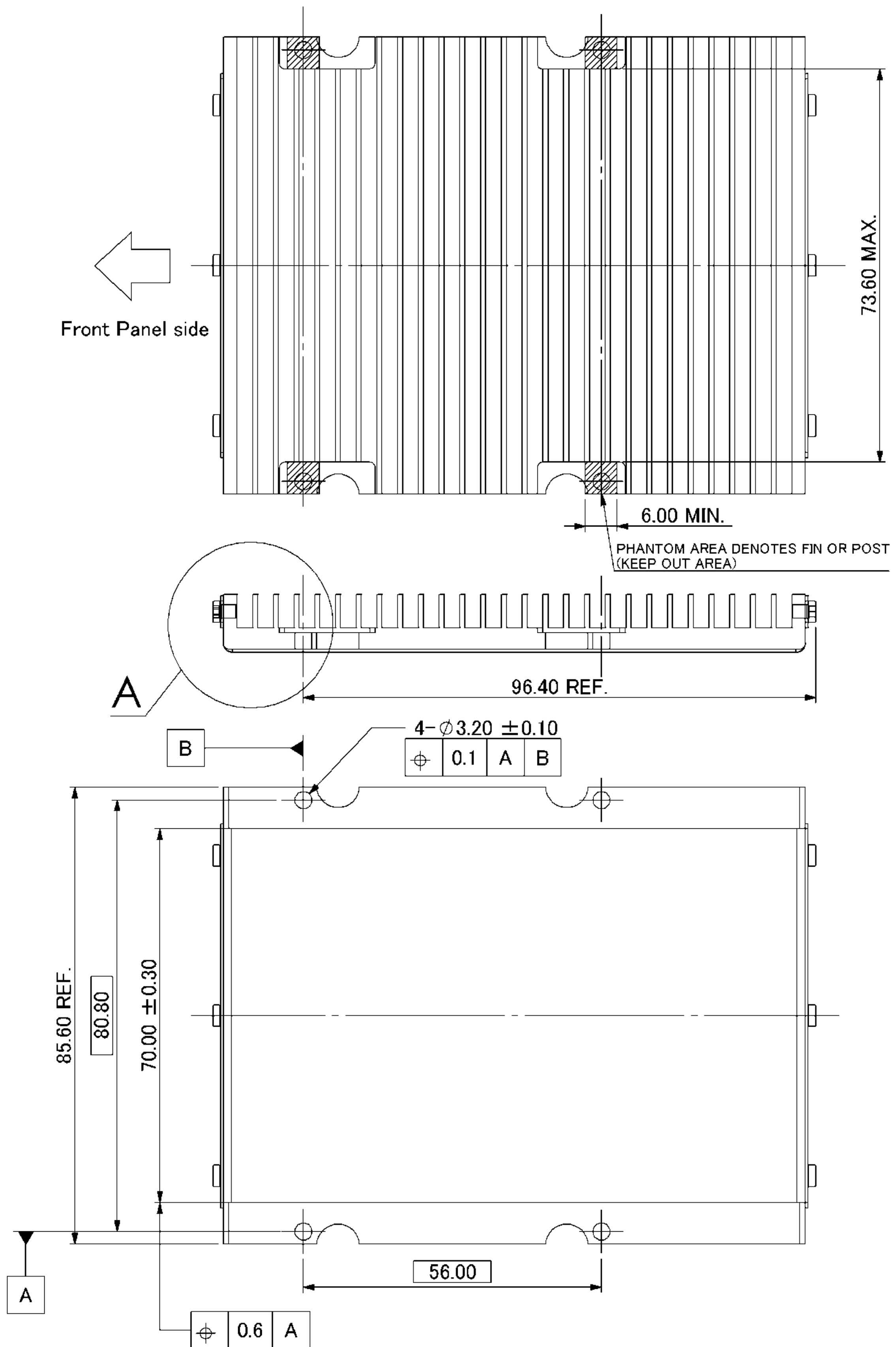


Figure 5-12: Riding Heat Sink Detail A

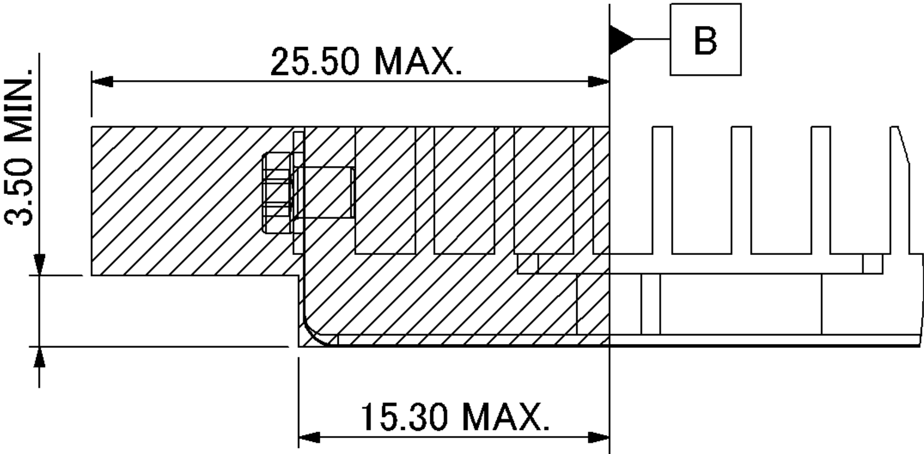
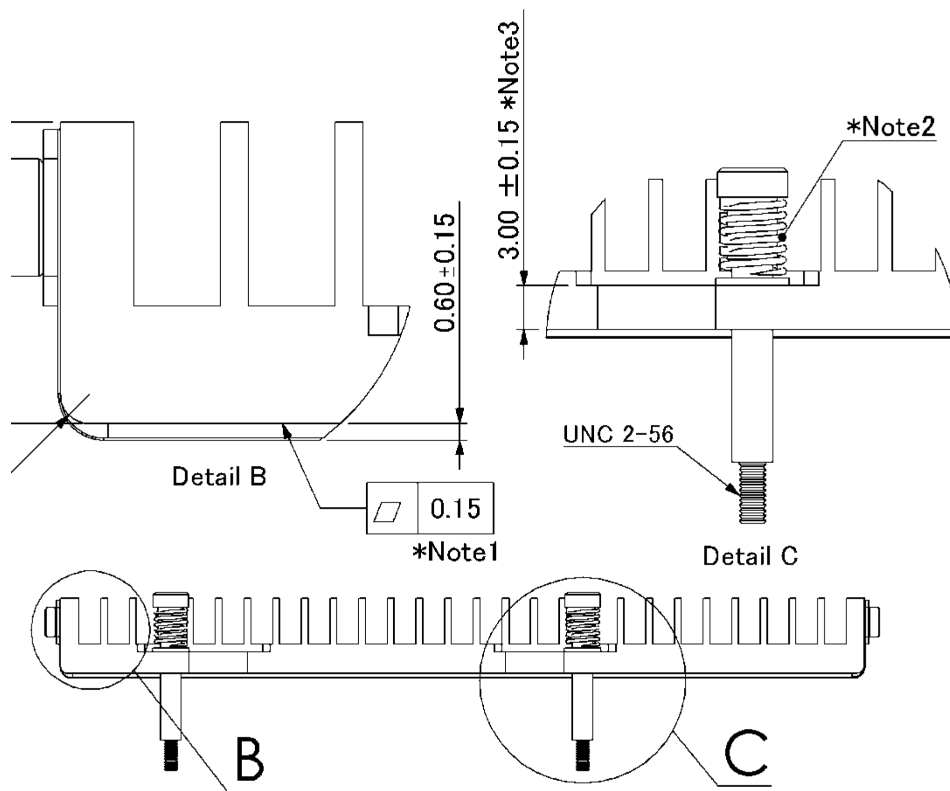


Figure 5-13: Riding Heat Sink Detail B & C[15,16,17]



[15] Note 1: Detailed co planarity requirement of thermal interposer is not specified. This plane is the base of the heat sink body and is sitting plane with the guide rail assembly top surface.

[16] Note 2: Each spring applies 2.5-3.75N(Total:10-15N) force to the module regardless of the orientation of the host board. This pressure calculation assumes the weight of the heat sink.

[17] Note3: A reference heat sink base thickness is 3mm

Figure 5-14: Riding Heat Sink Mounted on Guide Rail Assembly

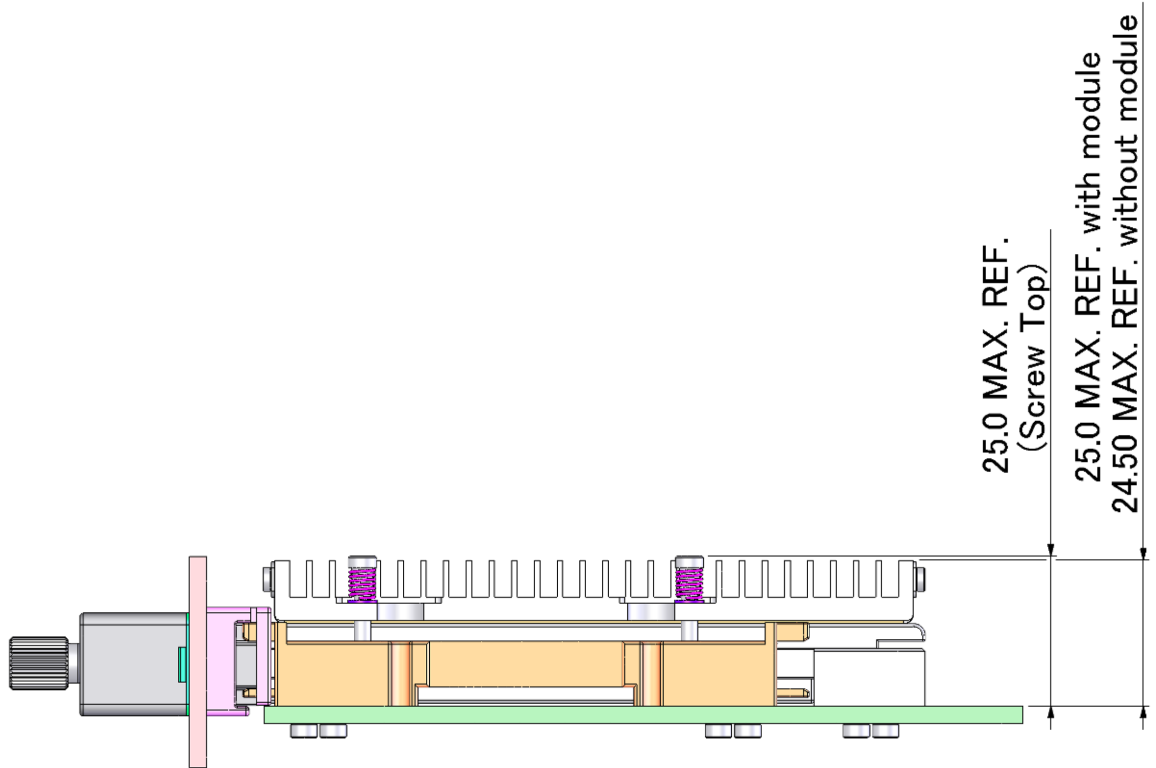
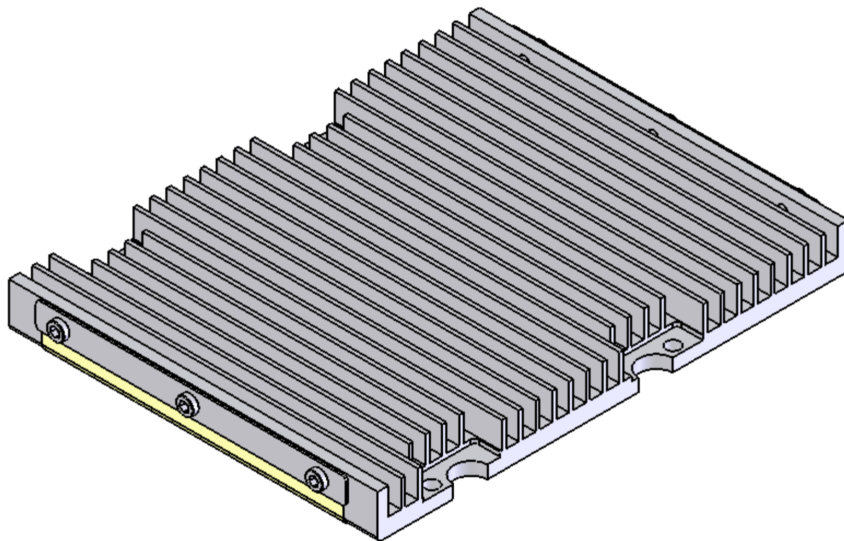


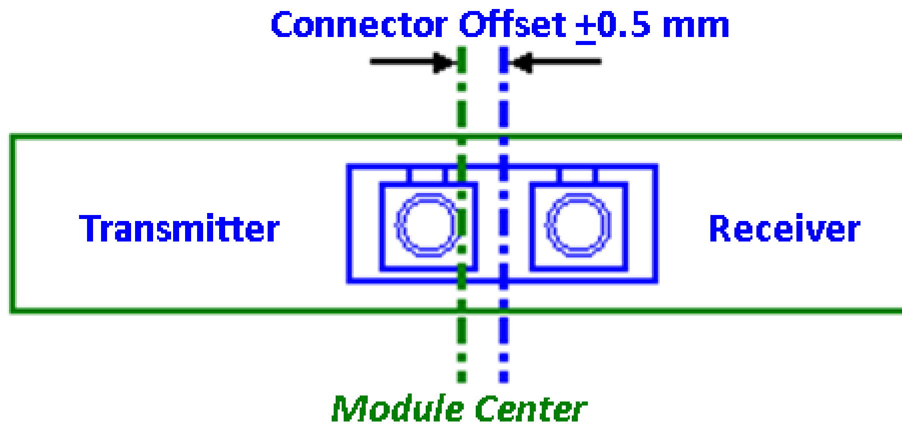
Figure 5-15: Riding Heat Sink Assembly



5.6 Optical Connectors

The optical connector for the MSA shall be located per Figure 5-16 below. The optical connector is centered in position along the X-axis (module width) with an offset tolerance of ±0.5mm. The position of the optical connector in the Y and Z axes shall be specified by the CFP module manufacturer.

Figure 5-16: CFP Optical Connector Position



5.6.1 Optional Optical LC Connector Position for Telecom Applications

Some telecom applications require adherence to a Network Equipment Building System standard such as, [12] NEBS Requirements: Physical Protection; Document Number GR-63. For such applications, an alternate optional configuration of the optical connector may be supported. A reference figure for such an application is shown below in Figure 5-17.

Figure 5-17: Optional Positioning for LC Connector CFP MSA modules

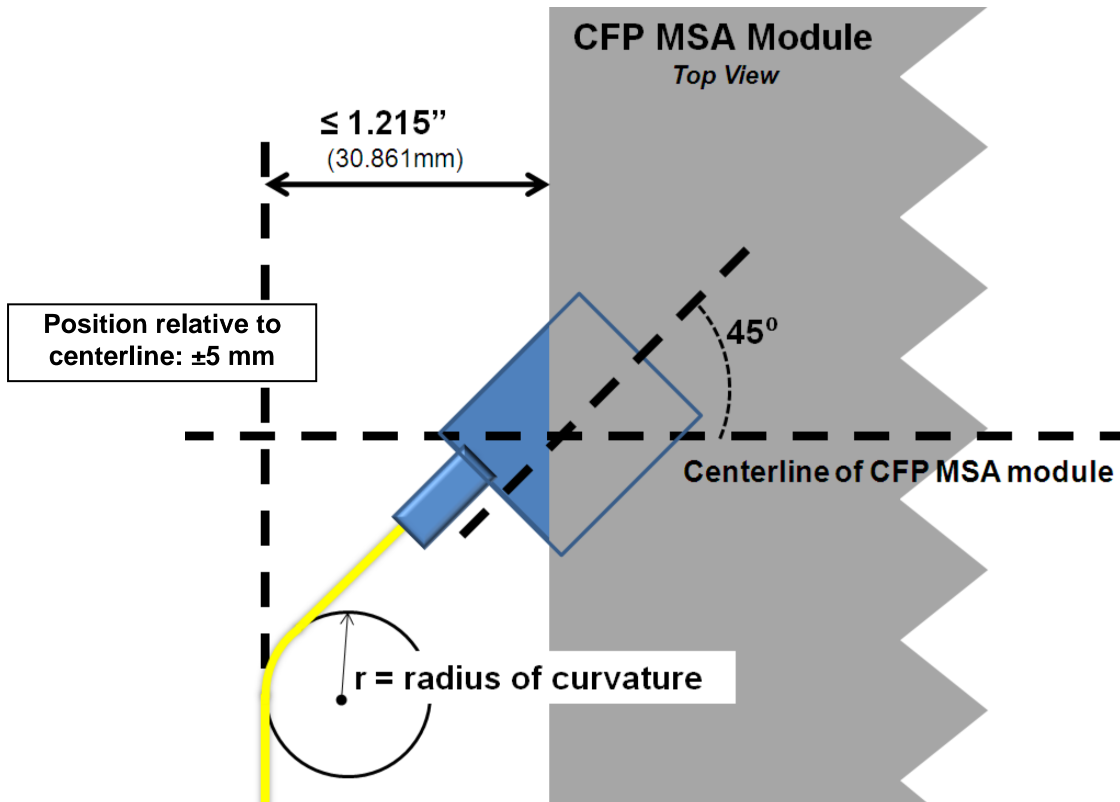


Table 5-3 Optical Connectors[18]

Pin #	Category	Reference Number
SC Connector		
LC Connector		
MPO Connector		

5.7 Electrical Connectors

Table 5-4 CFP MSA Host Connector Assembly (Tyco)

Part Number	Supplier	Part Name
2057626-1	Tyco Electronics	External Bracket Assembly
2057592-2	Tyco Electronics	Guide Rail
2057631-1	Tyco Electronics	Host Connector Cover Assembly
2057930-1	Tyco Electronics	Backer Plate Assembly
2057630-1	Tyco Electronics	Host Connector

Table 5-5 CFP MSA Host Connector Assembly (Yamaichi)

Part Number	Supplier	Part Name
CA009-1203-001	Yamaichi Electronics	External Bracket Assembly
CA009-1201-001	Yamaichi Electronics	Guide Rail
CA009-1400-001	Yamaichi Electronics	Host Connector Cover Assembly
CA009-1204-001	Yamaichi Electronics	Backer Plate Assembly
CA009-S001-001	Yamaichi Electronics	Host Connector

[18] Other optical connectors may be supported

5.8 Pin Assignment

The CFP connector has 148 pins which are arranged in Top and Bottom rows. The pin map is shown in Table 5-6 below. The detailed description of the Bottom row ranges from pin 1 through pin 74 and is shown Table 5-7 in below. The pin orientation is shown below in Figure 5-18.

Figure 5-18: CFP Pin Map Orientation

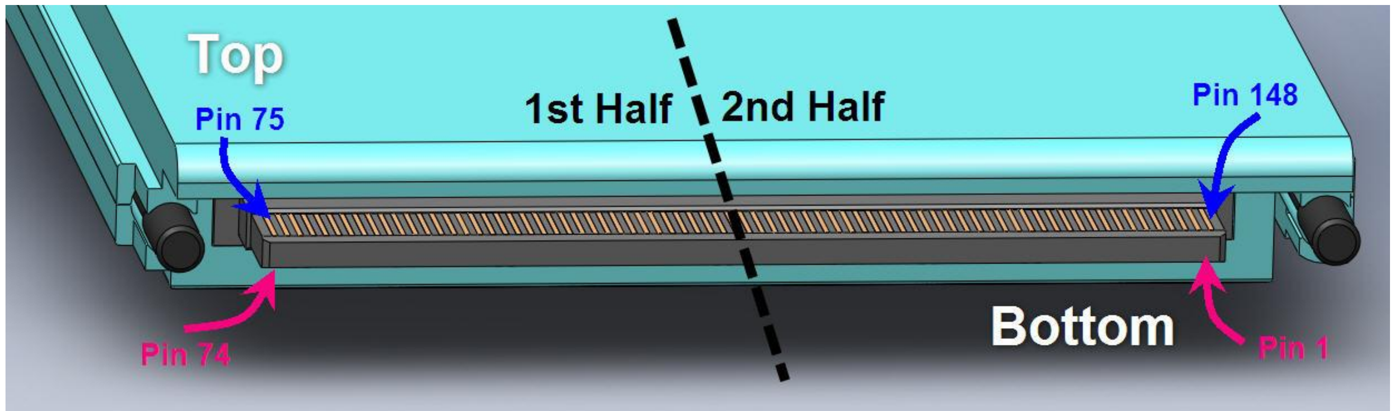


Table 5-6: CFP Pin-Map

	Top Row (2nd Half)		Bottom Row (2nd Half)		Top Row (1st Half)		Bottom Row (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	*N.C.*	39	MOD_RSTn
146	REFCLKp	3	3.3V_GND	109	*N.C.*	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	*N.C.*	5	3.3V_GND	107	RX9n	42	PRTADR4
143	*N.C.*	6	3.3V	106	RX9p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	TX9n	8	3.3V	104	RX8n	45	PRTADR1
140	TX9p	9	3.3V	103	RX8p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	TX8n	11	3.3V	101	RX7n	48	MDC
137	TX8p	12	3.3V	100	RX7p	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	TX7n	14	3.3V	98	RX6n	51	VND_IO_G
134	TX7p	15	3.3V	97	RX6p	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	TX6n	17	3.3V_GND	95	RX5n	54	VND_IO_J
131	TX6p	18	3.3V_GND	94	RX5p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	TX5n	20	3.3V_GND	92	RX4n	57	3.3V_GND
128	TX5p	21	VND_IO_A	91	RX4p	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	TX4n	23	GND	89	RX3n	60	3.3V
125	TX4p	24	*(TX_MCLKn)*	88	RX3p	61	3.3V
124	GND	25	*(TX_MCLKp)*	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	*(RX_MCLKn)*	72	3.3V_GND
113	TX0p	36	TX_DIS	76	*(RX_MCLKp)*	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Table 5-7: Bottom Row Pin Description

PIN #	NAME	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			
8	3.3V			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V			
14	3.3V			
15	3.3V			
16	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
22	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
23	GND			
24	*(TX_MCLKn)*	O	CML	For optical waveform testing. Not for normal use.
25	*(TX_MCLKp)*	O	CML	For optical waveform testing. Not for normal use.
26	GND			
27	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
28	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
29	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
30	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
32	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤8W, "01": ≤16W, "10": ≤24W, "11" or NC: ≤32W = not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
42	PRTADR4	I	1.2V CMOS	MDIO Physical Port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO Physical Port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO Physical Port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O F. Do Not Connect!
51	VND_IO_G	I/O		Module Vendor I/O G. Do Not Connect!
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do Not Connect!
54	VND_IO_J	I/O		Module Vendor I/O J. Do Not Connect!
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			

PIN #	NAME	I/O	Logic	Description
57	3.3V_GND			
58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			
62	3.3V			
63	3.3V			
64	3.3V			
65	3.3V			
66	3.3V			
67	3.3V			
68	3.3V			
69	3.3V			
70	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

6 Pin Map for Multi-Port 40Gbit/s Interfaces

Table 6-1: Pin-map for 1x40 and 2x40Gbit/s Applications

	Top Row (2nd Half)		Bottom Row (2nd Half)		Top Row (1st Half)		Bottom Row (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	*(S1_RX_MCLKn)*	39	MOD_RSTn
146	REFCLKp	3	3.3V_GND	109	*(S1_RX_MCLKp)*	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	*(S1_REFCLKn)*	5	3.3V_GND	107	*N.C.*	42	PRTADR4
143	*(S1_REFCLKp)*	6	3.3V	106	*N.C.*	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	*N.C.*	8	3.3V	104	*(S1_RX3n)*	45	PRTADR1
140	*N.C.*	9	3.3V	103	*(S1_RX3p)*	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	*(S1_TX3n)*	11	3.3V	101	*(S1_RX2n)*	48	MDC
137	*(S1_TX3p)*	12	3.3V	100	*(S1_RX2p)*	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	*(S1_TX2n)*	14	3.3V	98	*(S1_RX1n)*	51	VND_IO_G
134	*(S1_TX2p)*	15	3.3V	97	*(S1_RX1p)*	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	*(S1_TX1n)*	17	3.3V_GND	95	*(S1_RX0n)*	54	VND_IO_J
131	*(S1_TX1p)*	18	3.3V_GND	94	*(S1_RX0p)*	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	*(S1_TX0n)*	20	3.3V_GND	92	*N.C.*	57	3.3V_GND
128	*(S1_TX0p)*	21	VND_IO_A	91	*N.C.*	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	*N.C.*	23	GND	89	RX3n	60	3.3V
125	*N.C.*	24	*(TX_MCLKn)*	88	RX3p	61	3.3V
124	GND	25	*(TX_MCLKp)*	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	*(RX_MCLKn)*	72	3.3V_GND
113	TX0p	36	TX_DIS	76	*(RX_MCLKp)*	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Bottom row pin description is same as specified in Table 5-7.

Table 6-2: Pin-map for 3x40Gbit/s Applications

	Top Row (2nd Half)		Bottom Row (2nd Half)		Top Row (1st Half)		Bottom Row (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	S2_TX0n	2	3.3V_GND	110	S2_RX3n	39	MOD_RSTn
146	S2_TX0p	3	3.3V_GND	109	S2_RX3p	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	S2_TX3n	5	3.3V_GND	107	S2_RX2n	42	PRTADR4
143	S2_TX3p	6	3.3V	106	S2_RX2p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	S2_TX2n	8	3.3V	104	S1_RX3n	45	PRTADR1
140	S2_TX2p	9	3.3V	103	S1_RX3p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	S1_TX3n	11	3.3V	101	S1_RX2n	48	MDC
137	S1_TX3p	12	3.3V	100	S1_RX2p	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	S1_TX2n	14	3.3V	98	S1_RX1n	51	VND_IO_G
134	S1_TX2p	15	3.3V	97	S1_RX1p	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	S1_TX1n	17	3.3V_GND	95	S1_RX0n	54	VND_IO_J
131	S1_TX1p	18	3.3V_GND	94	S1_RX0p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	S1_TX0n	20	3.3V_GND	92	S2_RX1n	57	3.3V_GND
128	S1_TX0p	21	VND_IO_A	91	S2_RX1p	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	S2_TX1n	23	GND	89	RX3n	60	3.3V
125	S2_TX1p	24	(TX_MCLKn)	88	RX3p	61	3.3V
124	GND	25	(TX_MCLKp)	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	S2_RX0n	72	3.3V_GND
113	TX0p	36	TX_DIS	76	S2_RX0p	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Bottom row pin descriptions is same as in Table 5-7.

7 REGULATORY COMPLIANCE

7.1 Laser Safety

CFP MSA module manufacturer is responsible for the compliance to any laser safety regulations.

7.2 ESD/EMI/EMC

The CFP module and high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The CFP module and all host pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B.

The CFP module shall meet ESD requirement given in EN61000-4-2, criterion B test specification such that units are subjected to 15kV air discharges during operation and 8kV direct contact discharges to the case.

CFP MSA module manufacturer is responsible for the compliance to any electo-magnetic regulations.

7.3 Environment

CFP MSA module manufacturer is responsible for the compliance to any environmental regulations.

8 Appendix I: THERMAL DESIGN EXAMPLE

The following section provides thermal design reference for CFP MSA host system designers to model and characterize the thermal behavior of CFP modules.

The Riding Heat Sink system for the CFP MSA is a new design concept for optical modules and provides a high degree of flexibility in heat sink design. This flexibility enables host system designers to accommodate various power class CFP modules with various line card designs including dimensional variance or airflow variance. However, these varieties of heat sink system design will be supported by the heat sink systems manufacturer not by the CFP MSA.

8.1 Scope

The purpose of this section is to provide guidance to create a consistent test environment. This will identify the limiting boundary conditions to help the efficient thermal system design using CFP modules.

The parameters defined in this section shall enable clear communication of thermal simulation or thermal test data between module manufacturer and system vendor and will aid correlation between simulation and actual measured results.

This document however does not guarantee system level performance or port density. This will be resolved on a system specific basis. Any characterization results presented in this thermal section are given as examples only.

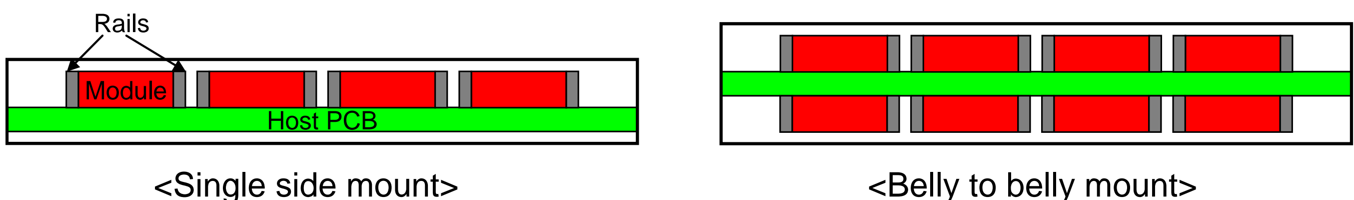
8.2 Riding heat sink system

The heat sink system for CFP modules introduces the “Riding heat sink system” whereby the heat sinks are attached on rails of a host card. As the CFP is inserted, the heat sink “rides” on top of the CFP module. This system allows the heat of the CFP module to be dissipated to the heat sink. The bottom of heat sink which “rides” on top of the CFP module shall have a low friction high thermal conductivity interface.

The Riding heat sink system enables system venders to design a common CFP port with a single faceplate aperture size. The optimum heat sink may be designed to accommodate the thermal management of various line card designs depending on the variation of the power class (defined in Table 8-1), line card dimension, module port number and air flow direction.
Below are examples.

1) For power class 1 (<8W, no riding heat sink is shown)

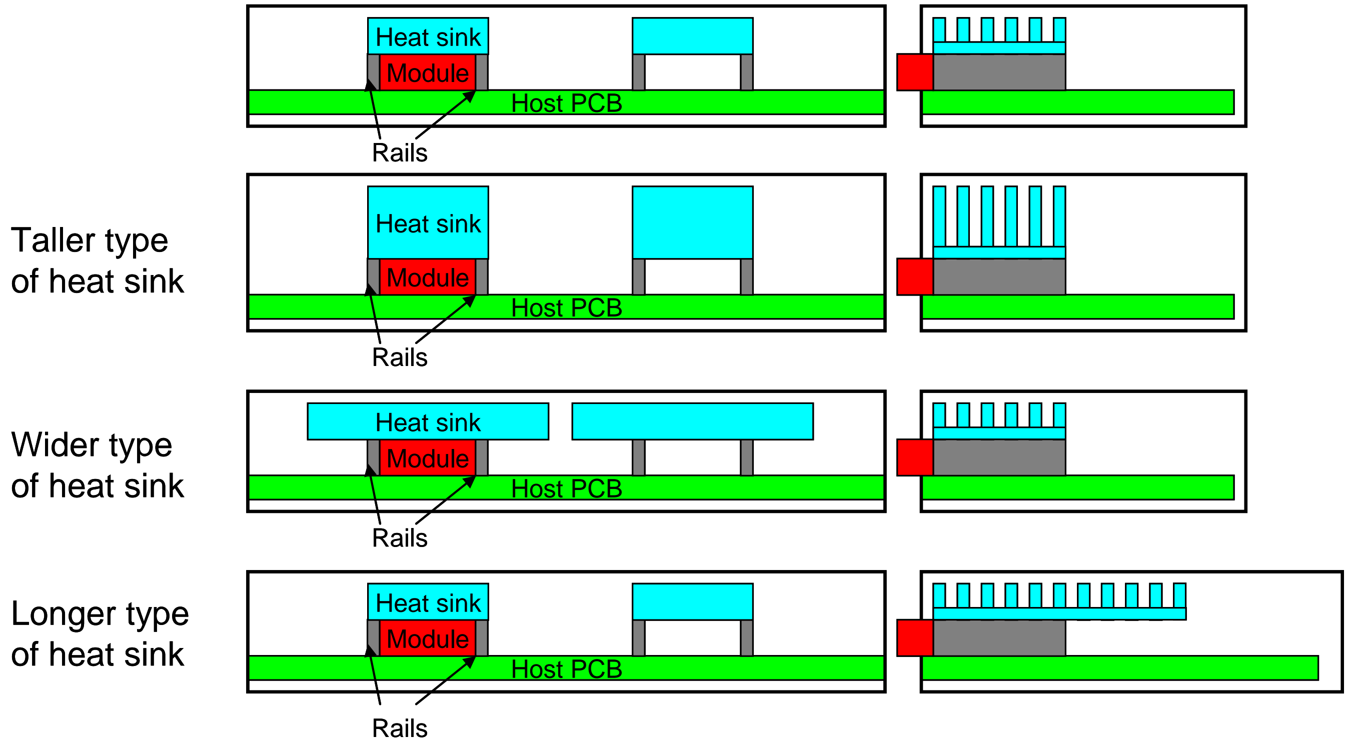
Figure 8-1: Mounting of CFP MSA module



<Single side mount> <Belly to belly mount>

2) For power class 2, 3, 4 (>8W, riding heat sink strongly recommended)

Figure 8-2: Example Riding Heat Sink Configurations



8.3 Assumption for thermal characterization and simulation

Information presented by the module vendor in relation to this document is obtained from a 'confined or ducted flow' described as:

- A wind tunnel is defined in Figure 8-3
- The multiple module configurations are defined in Table 8-1
- Test environment is shown in Table 8-2

Other assumptions:

- PCB host board has no copper layer.
- Duct housing is made of plastic.
- Dimensions of the chassis allow maximum 4 modules on 86.0 mm spacing.

Setup:

- Fans are arranged across the vent opening such that the direction of airflow is side to side (length axis) and be of constant volume airflow.
- Airflow is characterized using a calibrated hot wire anemometer placed at the airflow inlet.
- Thermocouples are used to measure the case temperatures
- Case temperature measurement point will vary by module vendor and PMD type. Module vendors may identify the information to the end user for verification in the system level environment.
- A steady state is obtained at measurements.

- Not all combinations of power classes nor heat sink sizes were considered for this characterization
- During thermal evaluation, CFP modules should handle the specified data patterns (TBD) on both the XLAUI/CAUI and PMD outputs.
- Other measurement data provided is at the discretion of the module manufacturer.

· An example of simulated and measurement data is shown in Figure 8-4.

Figure 8-3: Wind tunnel

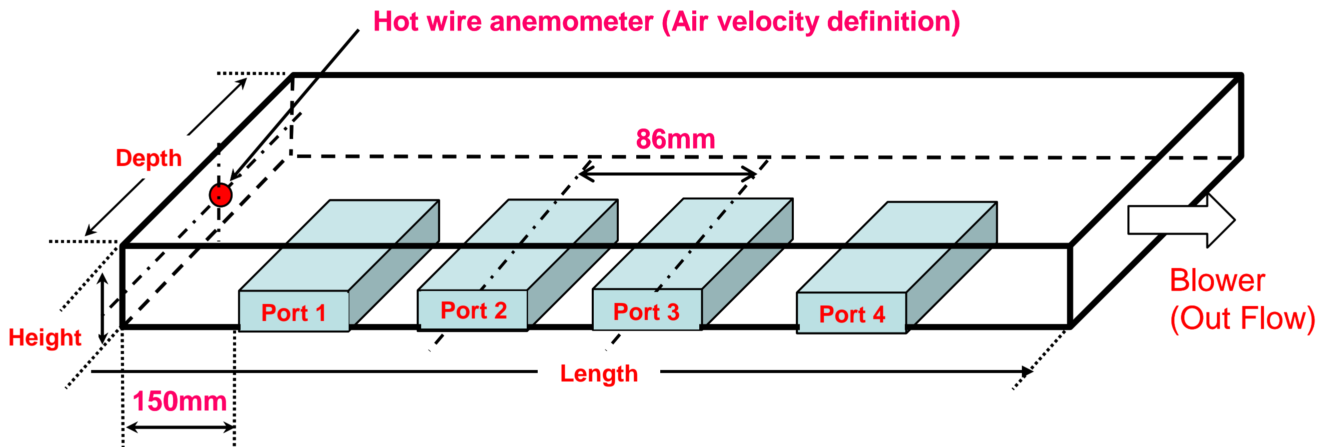


Table 8-1: Wind Tunnel Dimensions & Module Position[19], [20], [21]

Case	Heat Sink Type	Heat Sink Dimensions			Wind Tunnel Dimensions			Port 1	Port 2	Port 3	Port 4
		Height	Depth	Length (Width)	Height	Depth	Length				
1	No Riding Heat Sink	N/A	N/A	N/A	16.6	190	644	CFP 1	CFP 2	CFP 3	CFP 4
2	25.4mm Total Conformal	11.8	103	81	28.4	190	644	CFP 1	-	CFP 2	-
3	35mm Total Conformal	21.4	103	81	38	190	644	CFP 1	-	CFP 2	-
4	25.4mm Total & 105mm width	11.8	103	105	28.4	190	644	CFP 1	-	-	CFP 2
5	35mm Total & 210mm depth	21.4	185	81	38	260	644	CFP 1	-	CFP 2	-

[19] The Heat Sink height is simply a subtraction of the Total Height from the CFP module height. The heat sink fins will not be representative of this Heat Sink height number as a base thickness for the assembly is required.

[20] The Height of the wind tunnel refers to the allowable height for airflow – meaning from the top of the PCB surface

[21] Other heat sink dimensions may be investigated. The cases listed are only meant to be illustrative.

8.4 Preliminary Example Results

The purpose of this section is to provide a example test result for thermal testing of CFP modules in a host system. The test results shown in Figure 8-4 represent a no baffled airflow condition. During testing it was found that most of the airflow bypassed the CFP module heat sinks and was not effectively cooling the modules. Careful design of the heat sink and airflow is recommended for the host system design.

Table 8-2: Test Environment

Assumed airflow	200, 300, 400, 500 LFM
Altitude	Sea level
Air humidity	50% +/- 10%
Inlet Air temperature	0-50degC
CFP Configuration	Case 2; Table 8-1
Baffling	NONE

Figure 8-4: CFP Temperature Rise over Airflow (No Baffling Condition)